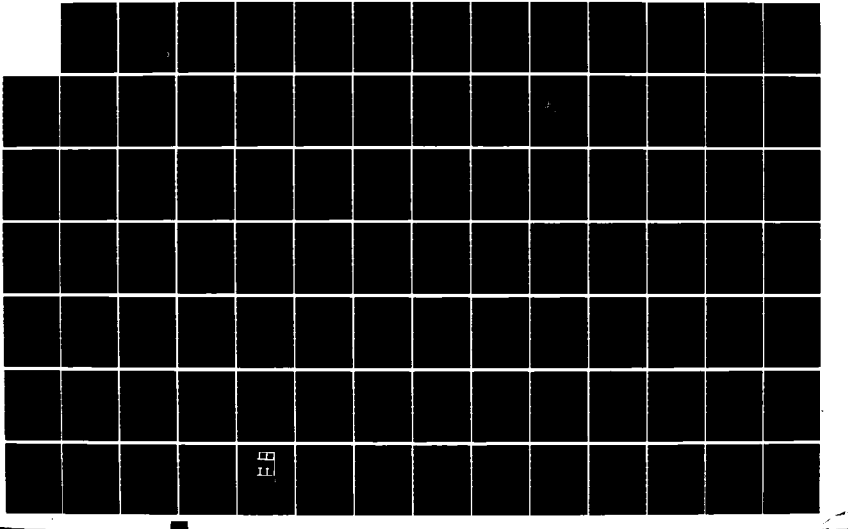
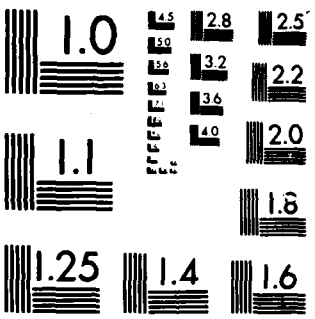
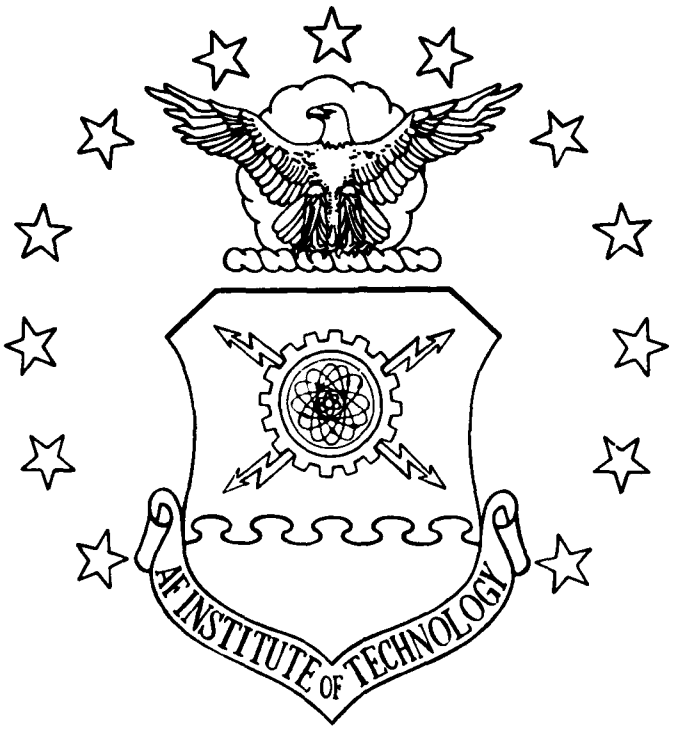
AD-A164 103 STUDY AND ANALYSIS OF ALGAAS/GAAS MODULATION DOPED FIELD-EFFECT TRANSISTO..(U) AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH SCHOOL OF ENGI.. K L PRIDDY 1/2

UNCLASSIFIED DEC 85 AFIT/GEO/ENG/85D-1 F/G 9/5 NL







STUDY AND ANALYSIS OF AlGaAs/GaAs MODULATION DOPED FIELD-EFFECT TRANSISTORS INCORPORATING P-TYPE SCHOTTKY GATE BARRIERS

THESIS

Kevin L. Priddy
First Lieutenant, USAF

AFIT/GEO/ENG/85D-1

DEPARTMENT OF THE AIR FORCE
AIR UNIVERSITY
AIR FORCE INSTITUTE OF TECHNOLOGY

Wright-Patterson Air Force Base, Ohio

AFIT/GEO/ENG/85D-1

STUDY AND ANALYSIS OF AlGaAs/GaAs MODULATION DOPED FIELD-EFFECT TRANSISTORS INCORPORATING P-TYPE SCHOTTKY GATE BARRIERS

THESIS

Kevin L. Priddy
First Lieutenant, USAF

AFIT/GEO/ENG/85D-1

Approved for public release; distribution unlimited

AFIT/GEO/ENG/85D-1

STUDY AND ANALYSIS OF AlGaAs/GaAs MODULATION DOPED FIELD EFFECT TRANSISTORS INCORPORATING P-TYPE SCHOTTKY GATE BARRIERS

THESIS

Presented to the Faculty of the School of Engineering

of the Air Force Institute of Technology

Air University

In Partial Fulfillment of the

Requirements for the Degree of

Master of Science in Electrical Engineering

Kevin L. Priddy, B.S.

First Lieutenant, USAF

December 1985

Preface

The enhanced Schottky barrier MODFET (ESMODFET) is presented and shown to increase the range of allowed gate voltages for the MODFET from the typical 0.8V up to 1.6V. This thesis expands the concept of Schottky barrier modification first proposed by Shannon and applies it directly to the MODFET.

I am deeply indebted to Dr. Hadis Morkoc, William Kopp, John Klem and Tim Henderson of the Coordinated Science Lab, University of Illinois, for the devices fabricated for this thesis. I also wish to thank Dr. Naresh Chand, Dr. Mike Moloney, Dr. George Norris, and Dr. Andy Ezis for their helpful discussions.

My special thanks are reserved for my thesis advisor Major Don Kitchen for his helpful guidance throughout this thesis and to Dr. Cole Litton who sponsored this project and offered many insights into the problems encountered. I also wish to thank Lieutenant Joe Grzyb who helped provide the equipment used for this thesis.

Last and most important of all, I wish to thank my wife Wendy for helping me to complete this work.

KEVIN PRIDDY

Table of Contents

	Page
Preface	ii
List of Figures	v
List of Tables	ix
Abstract	x
Notation	xi
I. Introduction	1-1
Motivation	1-1
Problem	1-3
Scope	1-3
Assumptions	1-4
Major Results	1-4
Sequence of Presentation	1-5
II. Theoretical Background	2-1
Molecular Beam Epitaxy	2-1
The Standard MODFET	2-4
Energy Bands	2-6
Two Dimensional Electron Gas	2-8
Electron Mobility	2-11
Schottky Barrier Modification	2-14
MODFET Modeling	2-18
Charge Control	2-18
Standard MODFET	2-18
Enhanced Schottky MODFET	2-20
Current Control	2-22
Transconductance	2-26
Small Signal Gate Capacitance	2-27
III. Equipment	3-1
Fabrication Equipment	3-1
Spinner	3-1
Mask Aligner	3-1
Pre-Bake Oven	3-1
Alloying Oven	3-2
Evaporation Chamber	3-2

		Page
	Test Equipment	3-3
	Current Source	3-3
	Digital Multimeter	3-3
	Semiconductor Parameter Analyzer	3-3
IV.	Experimental Design	4-1
	Layer Thickness Design	4-1
	Enhancement Devices ($V_{off}>0$)	4-1
	Depletion Devices ($V_{off}<0$)	4-4
	Device Fabrication	4-9
V.	Experimental Results	5-1
	Schottky Barrier Modification	5-1
	Turn-on Voltage	5-2
	Transconductance	5-4
	Resistance Measurements	5-4
	Ohmic Contact Measurement	5-8
VI.	Discussion of Results	6-1
	Schottky Barrier Height	6-1
	Effective Doping Concentration	6-10
	Turn-on Voltage	6-11
	Fabrication	6-12
VII.	Conclusions and Recommendations	7-1
	Conclusions	7-1
	Recommendations	7-2
Appendix A:	Derivation of Barrier Height for Metal-p+(GaAs)-n(AlGaAs) System from Poisson's Equation	A-1
Appendix B:	Derivation of Schottky Barrier Height for the ESMODFET from Poisson's Equation	B-1
Appendix C:	Fabrication Procedure for ESMODFETs	C-1
Appendix D:	Transistor Characteristics	D-1
Bibliography		BIB-1
Vita		vita

List of Figures

Figure		Page
1-1.	MESFET and MODFET Structures	1-2
2-1.	Typical MBE System	2-2
2-2.	Typical MODFET Structure	2-5
2-3.	Bandgaps of AlGaAs and GaAs Before the . . . . Heterojunction is Formed	2-7
2-4.	Energy Band Diagram of an AlGaAs/GaAs Junction Showing the Depletion Layer in the AlGaAs Caused by the Migration of Electrons Into The Potential Well	2-7
2-5.	Conduction Band Edge Diagram For The MODFET. . After The Gate is Added	2-9
2-6.	2DEG Carrier Density vs Depth into the GaAs. . Buffer Layer	2-10
2-7.	Physical Dimensions of 2DEG for MODFET	2-10
2-8.	Electron Mobility vs AlAs Mole Fraction. . . . For Various Temperatures	2-13
2-9.	Conduction Band Diagram For Metal-p+-n . . . . System with Equal Bandgaps	2-15
2-10.	Conduction Band Diagram for Metal/p+ GaAs/ . . n-AlGaAs System with Different Bandgaps	2-17
2-11.	Conduction Band Diagram for ESMODFET	2-21
2-12.	Channel Voltage vs Distance for MODFET	2-23
2-13.	Two-Piece Model of Electron Velocity vs. . . . Electric Field	2-25
2-14.	Gate-to-Drain Capacitance vs Drain Voltage for Various Values of Normalized Gate Voltage	2-29
2-15.	Gate-to-Source Capacitance vs Drain Voltage for Various Values of Normalized Gate Voltage	2-30

Figure		Page
3-1.	HP 4145 Semiconductor Parameter Analyzer . . .	3-4
4-1.	Conduction Band Diagram for ESMODFET for . . . $V_{off} > 0$.	4-2
4-2.	Conduction Band Diagram for ESMODFET for . . . $V_{off} = 0$	4-6
4-3.	Conduction Band Diagram for $V_{max} = 1.2V$, . . . $V_{off} = -0.5V$ using the Approximation of Eq 4-1	4-8
4-4.	Fabrication Process for ESMODFET	4-10
5-1.	Gate I-V Curve for MODFET and ESMODFET . . . . Fabricated from Sample 2377	5-2
5-2.	I-V Curve Used to Determine V_{off} for . . . . . Sample 2377	5-3
5-3.	Transconductance vs Gate Voltage for Sample 2377	5-5
5-4.	Circuit Diagram for Source Resistance. . . . . Measurement	5-6
5-5.	Drain I-V Characteristics for ESMODFET from. . Sample 2265	5-6
5-6.	Circuit Diagram for Combined Source and . . . Gate Resistance Measurement	5-8
5-7.	I-V Curve for a Pair of Contact Pads	5-10
6-1	Gate I-V for Two μm Devices on Sample 2377 .	6-2
6-2	Effect of Vds on Gate I-V Curves for . . . . . Sample 2265	6-5
6-3	Probe I-V Curve for Two Probe and Three. . . . Probe Measurements	6-6
6-4	Gate I-V Curve of MODFET and ESMODFET from . . Sample 2377	6-7
6-5	Drain Current vs Gate Voltage for MODFET from Sample 2377 Showing Shift when $V_g > V_b$	6-9

Figure		Page
6-6	Drain Current vs Gate Voltage for ESMODFET . . from Sample 2377 Showing Virtually No Shift	6-9
6-7	Effect of Slow Etchant on Ti Gate of ESMODFET	6-13
A-1	Metal-Semiconductor System of p+ MODFET . . .	A-2
A-2	Electric Field vs Position	A-3
B-1	ESMODFET Structure Under the Gate Contact. . .	B-2
B-2	Electric Field vs Position in ESMODFET	B-6
B-3	Electrostatic Potential vs Position for . . . ESMODFET	B-10
D-1	Gate I-V Curve for Sample 2263	D-2
D-2	Drain I-V Curve for Sample 2263.	D-3
D-3	Transconductance vs Gate Voltage for . . . . . Sample 2263	D-4
D-4	I-V Curve Used to Determine V_{off} for . . . . . Sample 2263	D-5
D-5	Gate I-V Curve for Sample 2265	D-6
D-6	Drain I-V Curve for Sample 2265.	D-7
D-7	Transconductance vs Gate Voltage for . . . . . Sample 2265	D-8
D-8	I-V Curve Used to Determine V_{off} for . . . . . Sample 2265	D-9
D-9	Gate I-V Curve for Sample 2373	D-10
D-10	Drain I-V Curve for Sample 2373.	D-11
D-11	Transconductance vs Gate Voltage for . . . . . Sample 2373	D-12
D-12	I-V Curve Used to Determine V_{off} for . . . . . Sample 2373	D-13
D-13	Gate I-V Curve for Sample 2376	D-14

Figure		Page
D-14	Drain I-V Curve for Sample 2376.	D-15
D-15	Transconductance vs Gate Voltage for Sample 2376	D-16
D-16	I-V Curve Used to Determine V_{off} for Sample 2376	D-17
D-17	Gate I-V Curve for Sample 2377	D-18
D-18	Drain I-V Curve for Sample 2377.	D-19
D-19	Transconductance vs Gate Voltage for Sample 2377	D-20
D-20	I-V Curve Used to Determine V_{off} for Sample 2377	D-21
D-21	Gate I-V Curve for Sample 2378	D-22
D-22	Drain I-V Curve for Sample 2378.	D-23
D-23	Transconductance vs Gate Voltage for Sample 2378	D-24
D-24	I-V Curve Used to Determine V_{off} for Sample 2378	D-25

List of Tables

Table		Page
2-1.	Semiconductor Materials Epitaxially Grown by Molecular Beam Epitaxy . . .	2-4
4-1.	Samples Used in Thesis	4-8
5-1.	Turn-on Voltage and Schottky Barrier Measurements for ESMODFET Samples	5-3
5-2.	Transconductance of ESMODFET Samples	5-5
5-3.	Resistance Values for ESMODFETs	5-7
5-4	Ohmic Contact Resistance Measurements	5-9
6-1	Measured Schottky Barriers Using Gate I-V . . .	6-2
6-2	Effective Doping Concentration	6-10

Abstract

The design and dc performance of enhanced Schottky barrier modulation doped field effect transistors (ESMODFETs) is presented. The theory required to estimate the layer thicknesses and dopings required for a desired barrier height is developed. The experimental results show an increase from 0.8eV to 1.6eV for the ESMODFET versus the standard MODFET with good correlation between theory and experiment. The ohmic contact resistance of the ESMODFET is shown to be comparable to that of the MODFET. The process used to fabricate the ESMODFET is similar to that used today for MODFETs.

Notation

Symbol	Definition
a	Slope of the linearized $E_f(n_s)$ function. (V/cm^2)
Δd	Effective depth of the two-dimensional electron gas in the quantum well. (Å)
d_d	Thickness of doped AlGaAs under gate. (Å)
d_i	Thickness of undoped AlGaAs under gate. (Å)
d	Total thickness of AlGaAs under gate. (Å)
E	Electric Field. (V/cm)
ΔE_c	Conduction band discontinuity at AlGaAs-GaAs heterojunctions. (0.811x V)
ΔE_g	Bandgap energy difference between GaAs and AlGaAs. (1.24x eV)
E_c	Conduction band energy level. (eV)
E_f	Fermi Level. (eV)
E_{fi}	Energy difference between Fermi level and the bottom of the triangular well. (eV)
E_{fo}	Zero intercept of linearized $E_f(n_s)$ function.(0V at 300K, 25mV at 77K)
E_g	Bandgap energy. (eV)
E_s	Saturation Electric field. (V/cm)
E_v	Valence band energy level. (eV)
E_1	Electric field in undoped AlGaAs under gate. (V/cm)
E_2	Electric field in doped AlGaAs under gate. (V/cm)
E_3	Electric field in p+ GaAs under gate. (V/cm)

Symbol	Definition
ϵ_0	Permittivity constant. (8.854×10^{-14} F/cm)
ϵ_1	Permittivity of GaAs. ($13.2\epsilon_0$)
ϵ_2	Permittivity of AlGaAs. ($(13.2-2.8x)\,\epsilon_0$)
g_m	Transconductance. (mS/mm)
g_m'	Intrinsic transconductance. (mS/mm)
I_g	Gate current. (mA)
I_d	Drain current. (mA)
k	Boltzmann's constant. (8.63×10^{-5} eV/molecule-K)
L	Gate Length. (μm)
μ	Electron Mobility. (cm^2/volt-sec)
N_a	Acceptor doping concentration.(cm^{-3})
N_d	Donor doping concentration. (cm^{-3})
N_s	Two-dimensional gas concentration. (cm^{-2})
ρ	Charge density. (cm^{-3})
q	Electronic charge. (1.602×10^{-19} coul)
R_c	Contact resistance. (Ω-mm)
R_d	Drain resistance. (Ω)
R_g	Gate resistance. (Ω)
R_s	Source resistance. (Ω)
R_{sd}	Combined source-drain resistance. (Ω)
R_{sg}	Combined source-gate resistance. (Ω)
ψ_1	Electrostatic potential in undoped AlGaAs under gate. (V)

Symbol	Definition
ψ_2	Electrostatic potential in doped AlGaAs under gate. (V)
ψ_3	Electrostatic potential in p+ GaAs under gate. (V)
t	Thickness of p+ GaAs layer. (Å)
V_b	Schottky barrier of gate metal to GaAs. (V)
V_g	Applied gate voltage. (V)
V_{max}	Modified Schottky barrier height. (V)
V_{off}	Turn-on voltage. (V)
W	Depletion width into AlGaAs. (Å)
Z	Gate Width. (μm)

STUDY AND ANALYSIS OF AlGaAs/GaAs MODULATION DOPED FIELD EFFECT TRANSISTORS INCORPORATING P-TYPE SCHOTTKY GATE BARRIERS

I. Introduction

Motivation

The modulation-doped field effect transistor (MODFET) is a high-speed transistor currently being studied by several corporations and universities. The MODFET is similar to the metal-semiconductor field effect transistor (MESFET), because both devices use the Schottky barrier formed by the gate contact (See Fig 1-1) to modulate the current in the device.

The Schottky barrier produced by the gate contact is dependent on the type of metal used, as well as the doping of the semiconductor. Many metals do not make good contacts with the semiconductor, which limits the range of possible barrier heights available to the transistor designer [57:1, 74:1004]. This thesis will explore alteration of the Schottky barrier through the use of highly-doped ultrathin p-type semiconductor layers under the gate contact. The additional barrier height obtained by using p+ surface layers will allow a larger gate voltage to be applied to the MODFET before the gate leakage current becomes excessive. The typical metal contact (Al,Ti) used for the gate in MODFETs has a Schottky barrier of around 0.8eV [74], while the Schottky barrier available from using p+ GaAs layers is that of the AlGaAs band-

gap, approximately 1.6eV for an Al mole fraction of 30 percent. The p+ MODFET, termed the enhanced Schottky MODFET (ESMODFET), can have any desired barrier between 0.8eV and 1.6eV through the use of the p+ GaAs semiconductor surface layer. While this thesis studies an aspect of the MODFET which has not been studied except by a few authors [40,52,64,65], the concept of using thin highly doped semiconductor layers to alter the Schottky barrier height of a metal-semiconductor junction has been around for several years [17,20,56,57,71]. The early work on Schottky barrier modification along with the theory developed for this thesis will be discussed in Chapter 2.

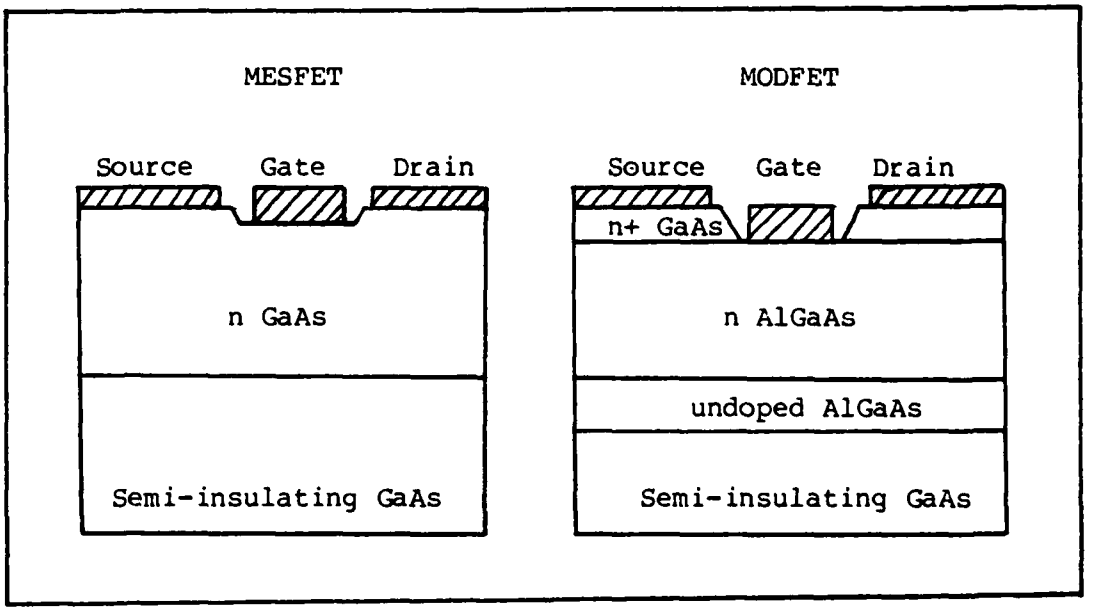


Fig 1-1. MESFET and MODFET Structures

Problem

The modification of Schottky barrier height by using highly doped semiconductor surface layers was first suggested by Shannon [57], and later shown to be valid for GaAs diodes by Eglash et al [17]. The addition of the p+ layer in the ESMODFET is a departure from previous fabrication procedures for the MODFET [18]. The charge control model developed by several authors [9,31,35,45,48, 49,54] must be modified to account for the p+ layer. The changes to the charge control model are significant in their impact, but blend easily into the standard MODFET model developed by Morkoc [49]. The modified charge control model can then be used to predict the threshold voltage (V_{off}), the transconductance (g_m), the capacitance, and the current-voltage (I-V) characteristics of the ESMODFET. Thus the problem is one of developing the model for the ESMODFET, determining the thickness and doping of each layer for a given V_{off} and enhanced Schottky barrier height (V_{max}), and finally altering the MODFET fabrication process to yield working ESMODFETs.

Scope

The scope of this thesis will be to develop a model to predict the I-V characteristics of the ESMODSFET, fabricate working devices, and then to test the devices and compare them to MODFETs with similar layer thicknesses to determine the advantages and disadvantages of the ESMODFET. The test measurements discussed in this thesis will be limited to the dc response of

the devices due to the limited amount of time that was available to fabricate and test the ESMODFET devices.

Assumptions

The assumptions used in this thesis are 1) that the pre sent model used by Morkoc [49] is correct, and 2) that the depletion approximation is valid for determining the charge relationships of the ESMODFET.

Major Results

ESMODFETs were fabricated with test results closely matching the predicted values from theory. The maximum available Schottky barrier for the ESMODFET is that of the bandgap of AlGaAs, which is approximately 1.6V for an Al mole fraction of 30 percent. The trans conductance of the ESMODFET is lower than that of a MODFET with a similar threshold voltage. The Schottky barrier was increased from 0.8eV to 1.62eV for ESMODFETs with 2μm gate lengths and a threshold voltage of -1.1V. The ease with which the Schottky barrier can be altered by the addition of the p+ layer is also a disadvantage due to the tight control required for layer thickness and doping. The slow etches typically used for the MODFET before applying the gate contact are not satisfactory for removing the p+ layer in the regions between the gate and source/drain for Ti gates because the metal is very reactive with the etchant [21,74:1003]. A GaAs selective etchant (NH_4OH:DI water: H_2O_2) buffered to pH 7.05 [18:306,Appendix C] worked best for removal of the p+ layer, despite the fact that the strength

of the etchant must be carefully controlled during preparation over a narrow range of pH values. This was because the required time of exposure to the selective etchant was much shorter than that of the slower etchant [Bell Labs proprietary] also used in the fabrication process.

Sequence of Presentation

Chapter 2 gives the theoretical background of the MODFET and introduces the theory of the ESMODFET, Schottky barrier contacts, and the charge control models used for both the MODFET and the ESMODFET. Chapter 3 describes the equipment used to fabricate and test the ESMODFET, while Chapter 4 outlines the experimental design of the ESMODFET. The test procedures used to measure the current-voltage (I-V) characteristics of the ESMODFET are given in Chapter 5. Chapter 6 summarizes the major test results and the corresponding match to the theory developed in chapter 2. Conclusions and suggestions for additional study on the ESMODFET are found in chapter 7.

II. Theoretical Background

The MODFET has a switching speed of less than 15 ps [18: 307, 32:19,46:28,58:352] while consuming less than 1 mW [18,37, 46]. The high speed of the MODFET is directly attributable to the unique way in which MODFETs are constructed. The MODFET is constructed with thin layers of dissimilar semiconductor material by a process known as molecular beam epitaxy (MBE) [59]. Other processes such as liquid phase epitaxy (LPE) [68] have been used to make heterostructures, but have proven to be less effective than MBE [39:43]. This chapter will discuss MBE, the MODFET, Schottky barrier modification, the ESMODFET, as well as introduce the theory of operation for the MODFET.

Molecular Beam Epitaxy

MBE permits the epitaxial growth of ultrathin semiconductor thicknesses with precise control over layer thicknesses down to a monolayer [39:44], which is about 2.8Å, as well as having the capability of producing extremely sharp doping profiles in layered semiconductor structures and junctions. Precise layer control is crucial to the operation of the MODFET as will be shown later. MBE is ideal for semiconductor fabrication because the layers created can be elemental semiconductors, compound semiconductors, or metals. Fig 2-1 is a picture of a typical MBE system [16:1381]. The MBE system consists of a high vacuum chamber (10^{-12} to 10^{-14} torr) [34,39], surrounded by a cyro shield through which liquid nitrogen flows, several molecular beam effusion cells, which

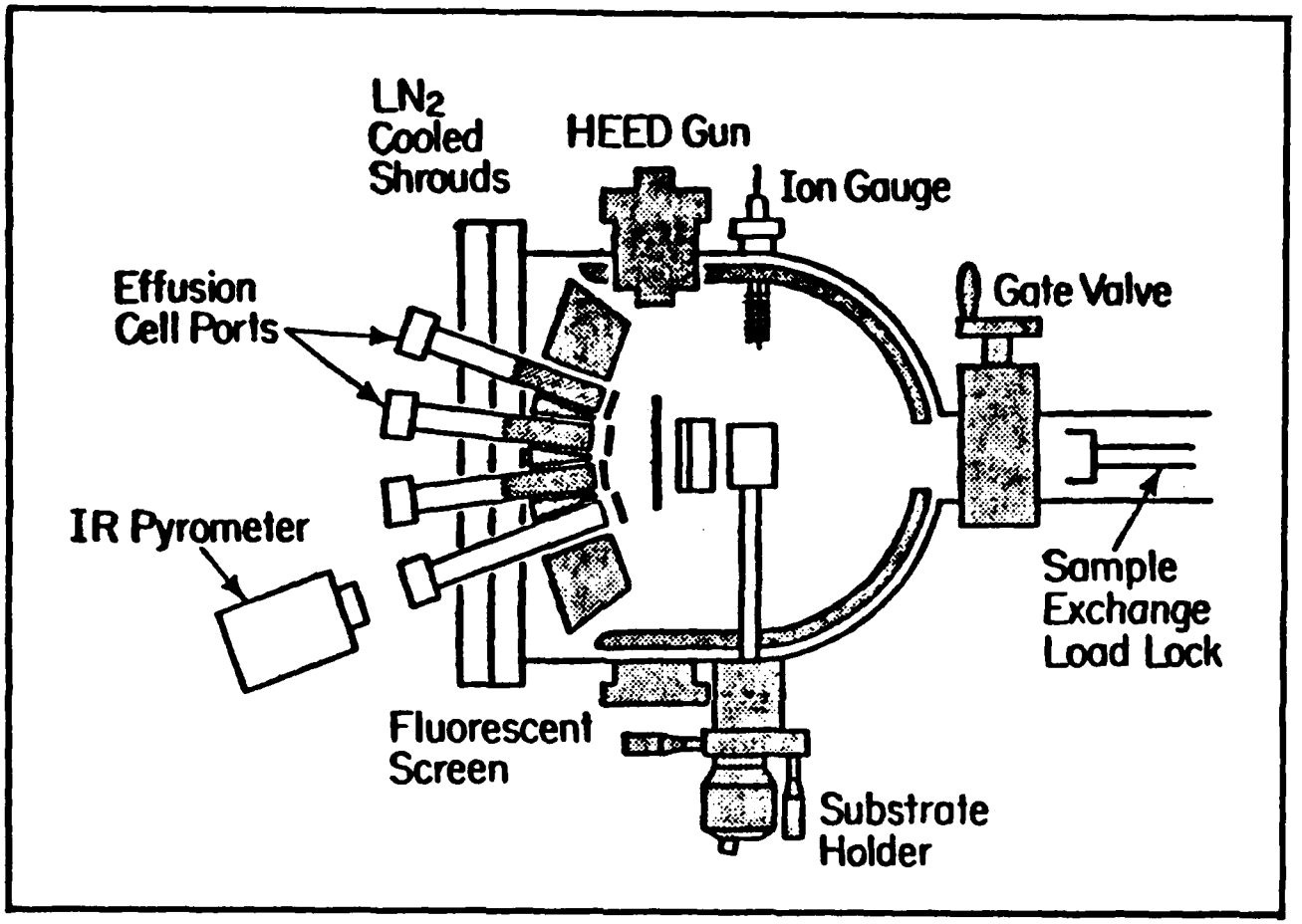


Fig 2-1. Typical MBE System [16]

direct molecular beams onto a crystalline substrate in the chamber, mechanical shutters which control the flux of the beams, and a heated crystal substrate holder which is used to hold the substrate upon which layers are grown. Some systems also have analytical devices such as reflection high energy electron diffraction (RHEED) guns to analyze the crystal surfaces being grown [38].

To produce a compound semiconductor such as GaAs, a combination of Ga and As molecular beams is used. When the molecular beams impinge upon a hot crystalline substrate, their molecular species undergo a kinetic reaction and chemisorb to the substrate surface. This process results in a monolayer by monolayer nucleation or growth of a single crystal layer upon the substrate surface [38]. If dopants are required during the process, a third source, consisting of the dopant, is used. Thus the growth of doped AlGaAs would require the use of four molecular beams. Most MBE systems have four or more effusion cells.

The semiconductor material grown by MBE can be very pure and virtually defect free [24], under controlled growth conditions. The purity and the perfection of the crystalline lattice strongly affect the mobility of free electrons in the semiconductor layers [14,32,72]. Table 1 shows the wide range of semiconductors which can be grown by MBE. With the wide range of semiconductor materials available from MBE, new devices such as the MODFET soon followed.

Table 1 Semiconductor Materials Epitaxially Grown by MBE [39]

III-V	IV-VI	II-VI	IV
GaAs	PbTe	ZnTe	Si
AlGaAs	PbSnTe	ZnSe	Ge
GaAsP	PbS	ZnSeTe	SiGe
InP	PbSe	CdTe	
InGaAs	PbSeSn	CdS	
GaSbAs	SnTe		
AlAs			

The Standard MODFET

The MODFET is fabricated from MBE semiconductor layers grown on a semi-insulating (SI) GaAs substrate (See Fig 2-2). Upon the SI substrate the following layers are grown in order: An undoped 1 μm layer of GaAs which is usually termed the buffer layer. This is followed by an undoped layer of AlGaAs (30-200)Å, the separation layer, upon which a doped layer (250-700)Å of AlGaAs is grown, and finally a GaAs capping layer (50-200)Å is grown on top of the doped AlGaAs layer. The source and drain contacts are made with a AuGeNi alloy, which is usually found to be necessary for the formation of ohmic contacts, while the gate is made with Al or a combination of Ti and then Au. In the case of Ti gates, Au is deposited upon the Ti to improve the ohmic conductivity of the gate contact.

The thickness of the separation layer affects the mobility of the MODFET [12,13,15,16,27,62,67]. Separation layers of 200A yield mobilities in excess of 10^6 $cm^2/V\text{-}s$ [24,59:1017]. Normally a thinner layer (20-30)Å is used to yield the best combina-

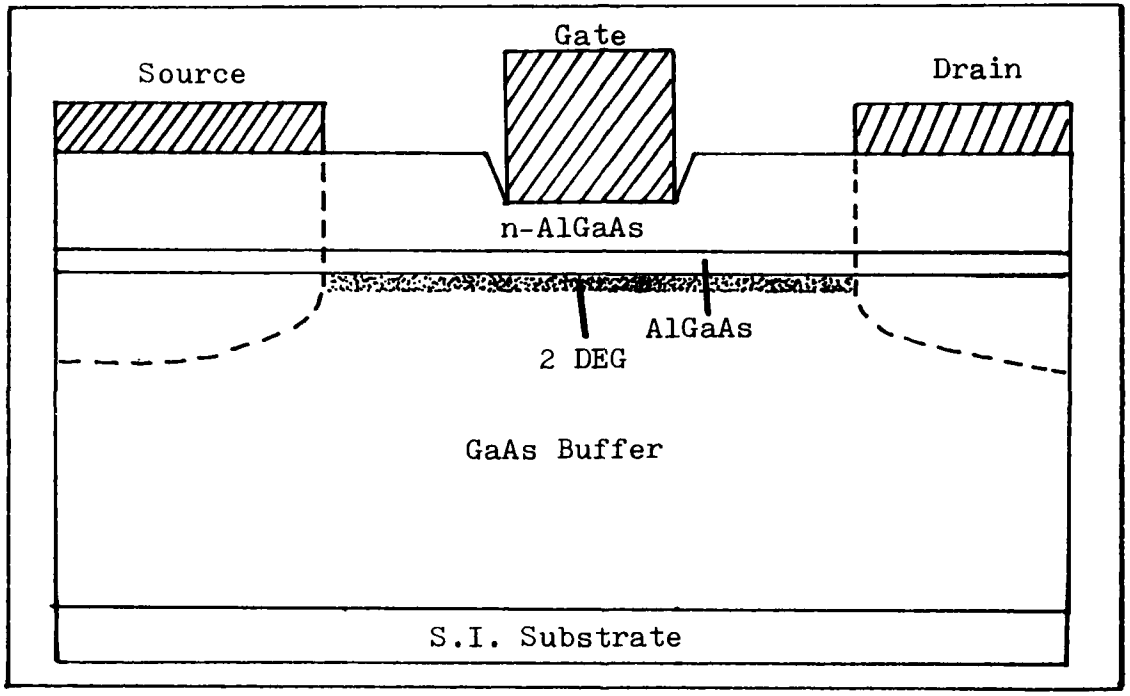


Fig 2-2. Typical MODFET Structure [59]

tion of speed and transconductance [59:1020].

The thickness and doping of the AlGaAs layer determines whether the device operates in the depletion-mode or in the enhancement-mode [46:32]. The thickness of the AlGaAs layer is determined by etching the layer until the desired threshold voltage (Voff) is obtained. The Ge in the AuGeNi alloy diffuses down into the undoped GaAs to provide an ohmic contact for the source and drain to the channel region of the MODFET [1,3,23,25,26,30,41,50,51,53,55]. The capping layer can be doped to alter the Schottky barrier height under the gate or to facilitate the formation of ohmic contacts in the source and drain regions [17,57,71].

The differing layers of the MODFET yield some unique properties which give the MODFET its tremendous speed. A better understanding of the MODFET is obtained by looking at the energy band structure for the various semiconductor layers.

Energy Bands. The operation of the MODFET depends on the properties of the AlGaAs/GaAs interface known as the heterojunction. To gain a better understanding of what happens at the interface one must look at the energy band diagrams of AlGaAs and GaAs (see Fig 2-3). The conduction band is labeled E_c, the valence band is labeled E_v, the bandgap is denoted by E_g, and the Fermi level is labeled E_f. As can be seen in Fig 2-3 the bandgap for AlGaAs is larger than that of GaAs. At the interface, according to semiconductor theory [43:390-393] the Fermi level must be continuous across the heterojunction interface. This results in bandbending as shown in Fig 2-4. The amount of bandbending is equal to the

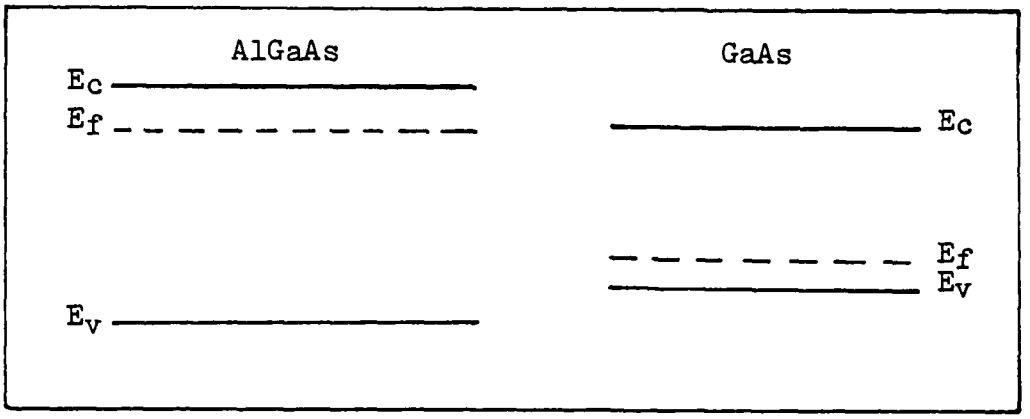


Fig 2-3. Bandgaps of AlGaAs and GaAs Before the Heterojunction is Formed

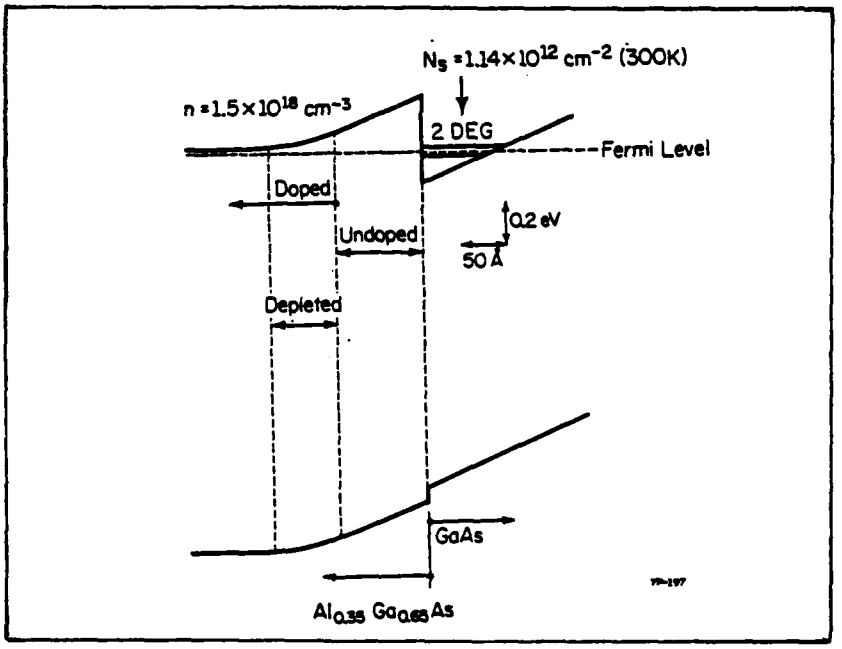


Fig 2-4 Energy Band Diagram of an AlGaAs/GaAs Junction Showing the Depletion Layer in the AlGaAs Caused by the Migration of Electrons into the Potential Well [64:II-9]

difference in conduction band energy (ΔE_c) between the two semiconductors. To return the system to equilibrium, electrons from the doped AlGaAs migrate to the undoped GaAs [46,48,59]. In the GaAs they are separated from their ionized donors, which are bound in the AlGaAs, and are prevented from returning by the potential difference ΔE_c. At room temperature, the potential ΔE_c is still much greater than kT, trapping the electrons in the GaAs. The result is an approximately triangular well which is formed in the conduction band of the GaAs [44:1226,59:1016,63:705]. When the gate is added, the band picture looks as shown in Fig 2-5. The addition of the gate has caused the conduction band to bend due to the barrier potential of the Schottky contact and the applied gate voltage. A negative gate voltage causes further bending, while a positive gate voltage lessens the band bending [54]. By controlling the Schottky barrier height and the gate voltage, the current in the MODFET can be varied. As will be shown later, the Schottky barrier and gate voltage have a direct effect on the number of electrons in the triangular well.

Two Dimensional Electron Gas. The electrons which are trapped in the GaAs form a quasi-two dimensional electron gas (2DEG) [33,34,44,46,63]. The triangular well (see Fig 2-4) is normally (50-100) A across, perpendicular to the heterojunction. The thin layer of carriers in the quantum well is shown in Fig 2-6 [44: L226]. Fig 2-6 is a comparison of the electron density with respect to distance into the GaAs from the heterojunction. As can be seen the electrons are confined in an 85Å thick layer close to

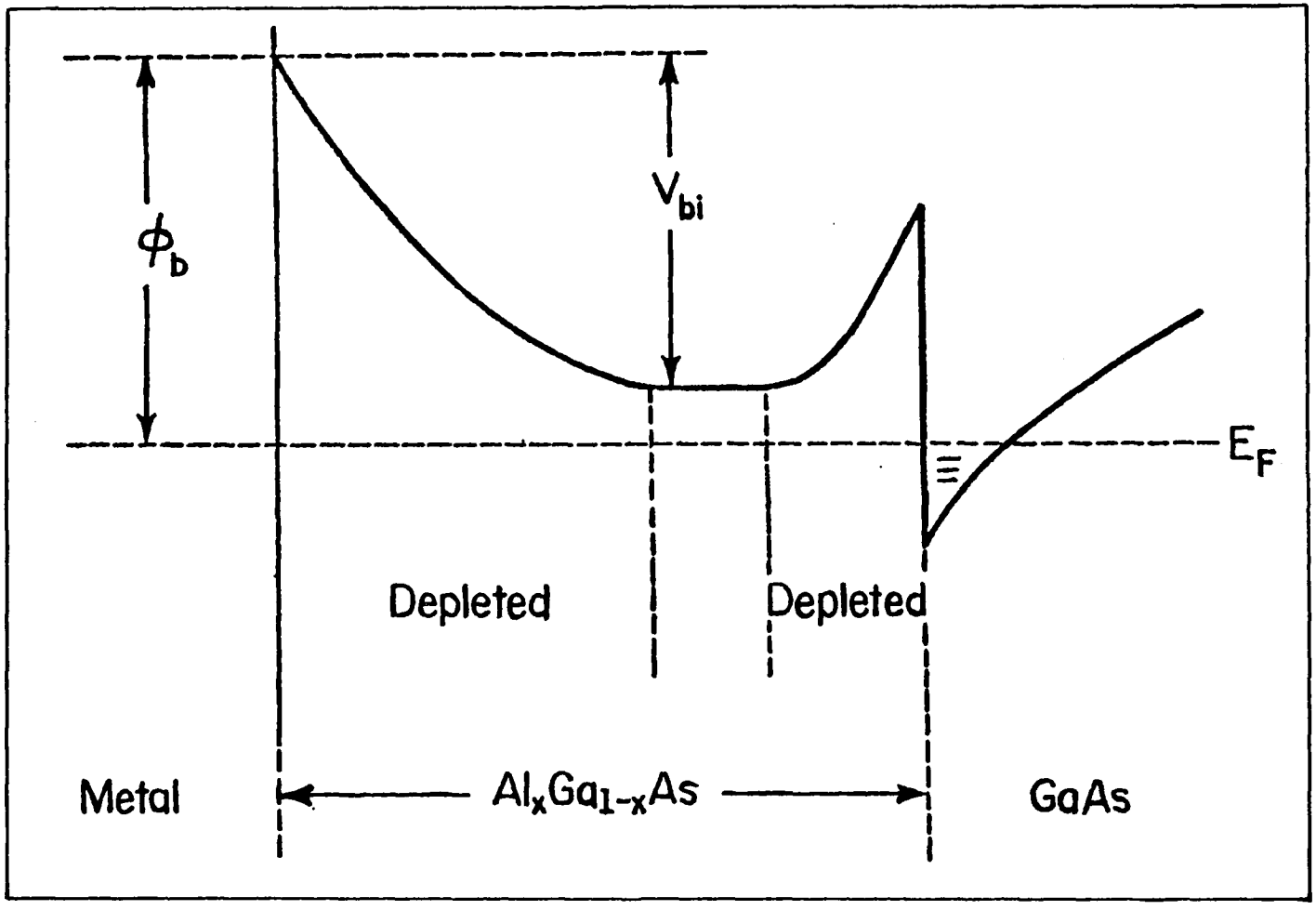


Fig 2-5. Conduction Band Diagram For The MODFET After The Gate is Added [49]

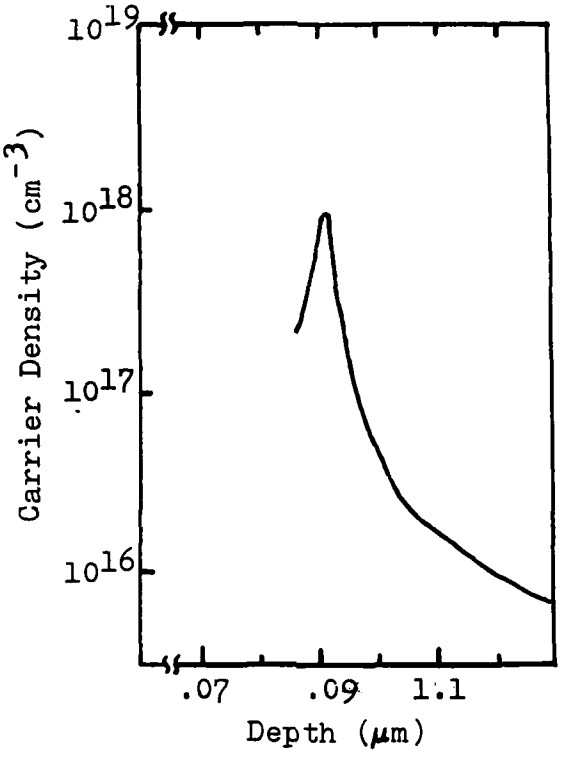


Fig 2-6. *2DEG Carrier Density vs Depth into* the GaAs Buffer Layer [19:L226]

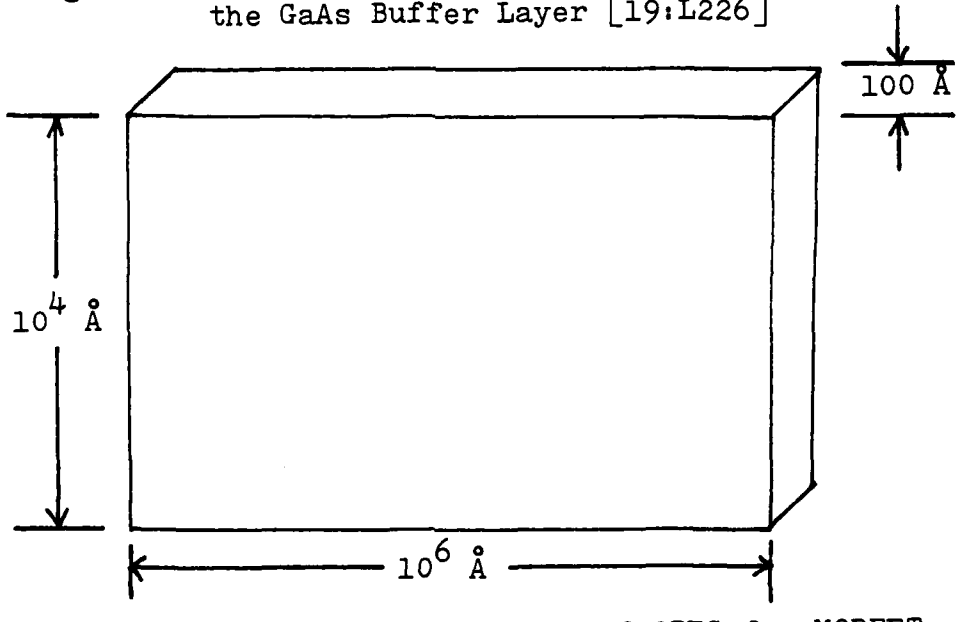


Fig 2-7. Physical Dimensions of 2DEG for MODFET

the heterojunction. The 2DEG approximation is derived from the dimensions of the MODFET. For a typical MODFET the gate length is 1 μm with a width of 25 to 300 μm. Thus the physical picture (see Fig 2-7) of the 2DEG is much like that of a sheet of paper. The thickness of the well is so small compared to its width or length, it is easier to describe it in two rather than three dimensions.

An actual quantum well is formed in the GaAs buffer layer because the electrons in the well are trapped by the potential barrier ΔE_c. By solving the Shroedinger wave equation, it can be shown that the only allowed states are quantized [61,73] with the ground subband containing 60% and the first subband 20% of the free electrons respectively, at room temperature [73:308]. The trapped electrons are no longer affected directly by the ionized donors due to the spatial separation caused by the potential barrier (ΔE_c), resulting in greatly increased mobility.

Electron Mobility. The mobility of the free electrons in the 2DEG is greatly enhanced due to their separation from the ionized donors in the AlGaAs. The main factors which affect mobility are coulombic scattering, acoustic phonon scattering due to lattice vibration, discontinuities in the crystal lattice, impurity scattering, and temperature [16,36,48:3-4,72]. Temperature is an important factor, because the amount of lattice vibration is directly proportional to the temperature of the crystalline substrate. The dominant scattering mechanism from room temperature down to 77 K is acoustic phonons [72:582]. Below 77 K the impurity scattering and coulombic scattering become important. Coulombic

scattering is due to the coulombic interaction between the free electrons and the ionized donors. Due to the separation of the electrons from the donors, coulombic scattering is nearly eliminated. The coulombic scattering can be reduced even further by increasing the thickness of the separation layer [12,15,16,27]. The GaAs layer grown by MBE is virtually free of lattice defects and unwanted impurities reducing the scattering due to impurities and lattice defects to very low levels. Thus, with a nearly perfect lattice structure and virtually no other scattering mechanisms present, the free electrons can attain very high mobilities as predicted from theory [43:208-216].

The mobility of the MODFET at room temperature is typically 8000 cm^2/volt-s with an increase to between 200,000 and 10^6 cm^2/volt-s below 77K [28,48:4]. The large difference in mobility at low temperatures is due to material constraints such as the thickness of the separation layer and the purity of the GaAs as well as the aluminum mole fraction in the AlGaAs [13,15,16]. Fig 2-8 gives the mobility of the electrons in the 2DEG versus the mole fraction of Al in AlGaAs with each curve representing a different temperature [16:1024]. As can be seen, the mobility goes up as the temperature is decreased. The ability to control the 2DEG with its associated mobility is made possible through the Schottky barrier formed by the gate contact. To better understand the operation of the MODFET and ESMODFET, the Schottky barrier and its associated theory will be introduced.

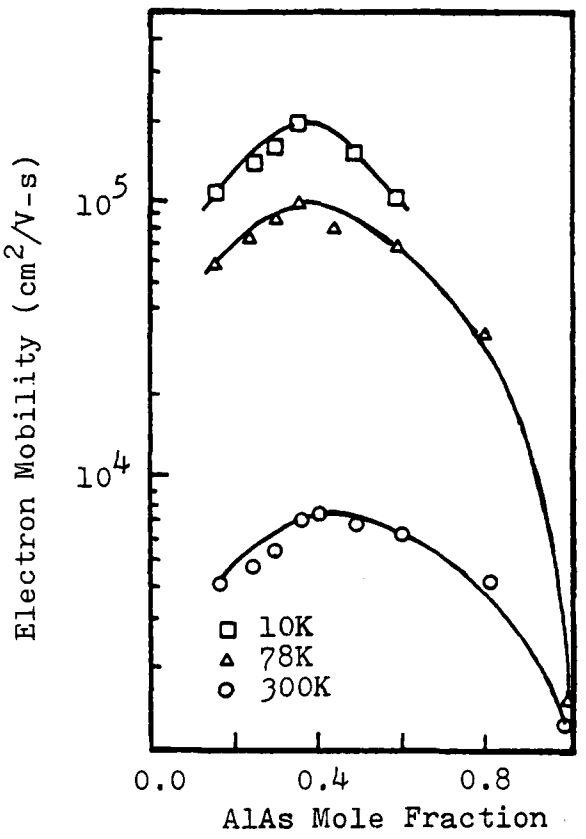


Fig 2-8. Electron Mobility vs AlAs Mole Fraction for Various Temperatures [21:1024]

Schottky Barrier Modification

In an ideal metal-semiconductor contact, the Schottky barrier is simply the difference between the electron affinity of the semiconductor and the work function of the metal. This barrier is dependent upon the work function of the metal and the surface states of the semiconductor. The barrier is fixed for a particular metal-semiconductor combination [17,57,74]. The height of the barrier can be altered by using various metals as contacts. Unfortunately, the range of possible Schottky barriers is limited for the available metals which make good physical contacts with semiconductors. Thus the available barriers available to the transistor designer are limited.

In 1976 Shannon [57] suggested that the Schottky barrier could be altered by using heavily-doped surface layers. Highly-doped n-type surface layers decrease the Schottky barrier, while highly-doped p-type surface layers increase the Schottky barrier [57:543]. Shannon's results were verified by Eglash et al [17] for GaAs diodes. The theory proposed by Shannon can also be applied to semiconductor surface layers with bandgaps which are different than the base semiconductor. The band diagram for a metal-p-n system is shown in Fig 2-9.

To obtain the band diagram, Poisson's equation must be solved in each region with the appropriate boundary conditions (see Appendix A). The boundary conditions used to obtain Fig 2-9 are that the electric field and the electrostatic potential must be continuous at x=W, and that the electrostatic potential is constant and

the electric field is zero at x=0. For simplicity the electrostatic potential was taken as zero at x=0. The actual value is dependent on the doping of the base semiconductor as well as the type of dopant used [19,69]. For highly-doped semiconductors the actual value is nearly zero.

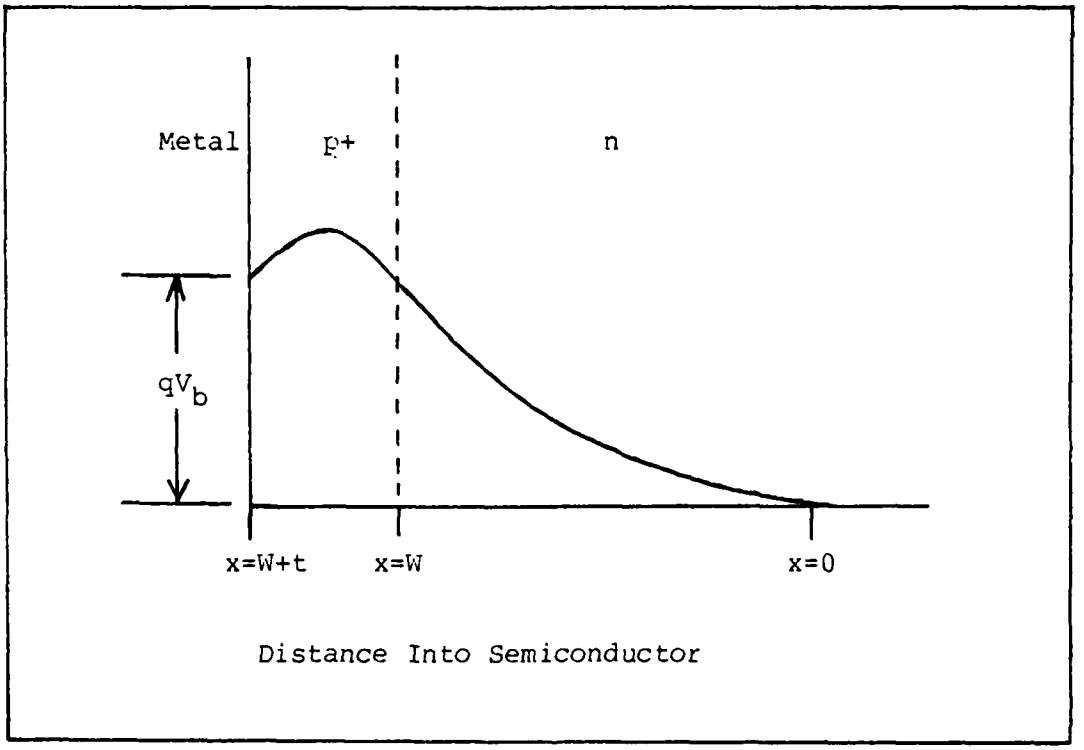


Fig 2-9 Conduction Band Diagram for metal-p+-n System with Equal Bandgaps.

The band diagram for the metal/p+ GaAs/n-AlGaAs system is given in Fig 2-10. The bandgap of AlGaAs is dependent on the mole-fraction of aluminum used [19:162,22]. The difference in conduction band energy (ΔE_c) is typically 65% of the total bandgap difference (ΔE_g) for mole-fractions less than 0.4

[22,54:1019]. The electrostatic potential as a function of distance is given by (see Appendix A)

$$\Psi(x) = \frac{qN_d x^2}{2\epsilon_2} \qquad (0 \le x \le W) \tag{2-1}$$

$$\Psi(x) = \frac{-qN_a(x-W)^2}{2\epsilon_1} + \frac{qN_d W^2}{2\epsilon_2} - \Delta E_c + \frac{qN_d W(x-W)}{\epsilon_1} \qquad (W \le x \le W+t) \tag{2-2}$$

where $\Psi(x)$ = electrostatic potential

x = position

t = p+ GaAs thickness

W = AlGaAs depletion depth.

N_d = doping of AlGaAs layer

N_a = doping of p+ GaAs layer

ϵ_2 = permittivity of AlGaAs

ϵ_1 = permittivity of GaAs

ΔE_c = conduction band discontinuity

The actual depletion depth into the AlGaAs (W) can be found by solving for W in the equation (See Appendix A)

$$V_b - V_g = \frac{-qN_a t^2}{2\epsilon_1} + \frac{qN_d W^2}{2\epsilon_1} + \frac{qN_d Wt}{\epsilon_1} - \Delta E_c \tag{2-3}$$

V_g = applied gate voltage

V_b = Schottky barrier of metal to p+ GaAs

which when rearranged yields

$$W = \frac{\epsilon_2 t}{\epsilon_1}\left[\left(1 + \frac{\epsilon_2 N_a}{\epsilon_1 N_d} + \frac{2\epsilon_1^2}{q N_d \epsilon_2 t^2}\left(V_b + \Delta E_c - V_g\right)\right)^{1/2} - 1\right] \quad (2\text{-}4)$$

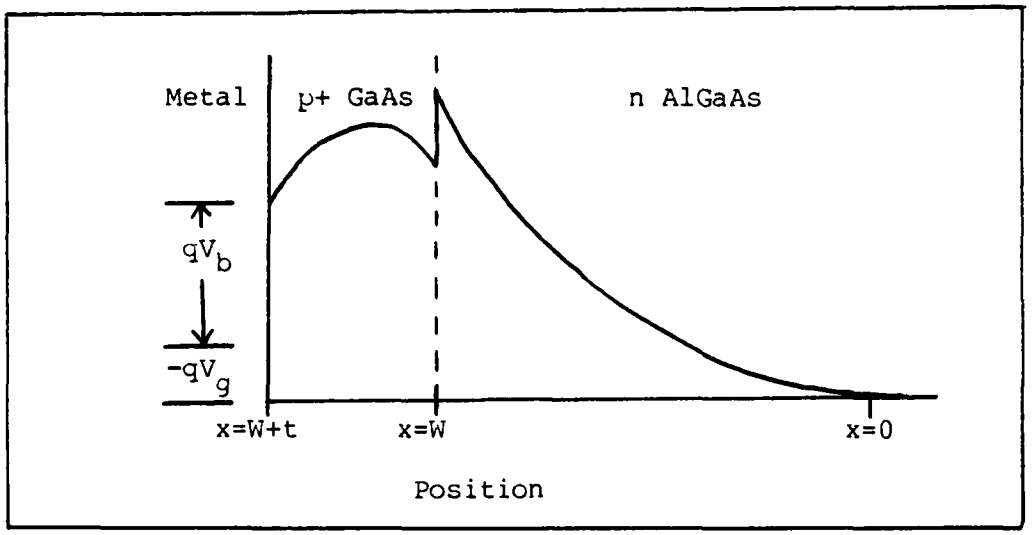


Fig 2-10 Conduction Band Diagram for Metal/p+ GaAs/ n-AlGaAs System with Different Bandgaps.

Thus, with a thorough understanding of the concept of barrier modification, the next step is to apply the concept of Schottky barrier modification to the MODFET. The band diagram of the MODFET and ESMODFET can be determined by solving Poisson's equation (see Appendix B) for each layer of the device. The charge control model developed for the MODFET is a result of the solution of Poisson's equation for the semiconductor interfaces of the MODFET. The charge control model is used to determine the relationship between device parameters such as layer thickness and doping to the electrical characteristics of the MODFET.

MODFET Modeling

The MODFET has been extensively modeled by several different authors [6,9,31,35,45,48,49,54]. This thesis will present the model developed by Morkoc and coworkers at the University of Illinois [48,54].

Charge Control. The thickness of the layers of the MODFET are tailored to provide an overlapping of the depletion due to the heterojunction and due to the gate contact and applied voltage. The amount of charge controlled by a given gate voltage can be predicted by analyzing the conduction band diagram of the MODFET.

Standard MODFET. The conduction band diagram of the standard MODFET is given in Fig 2-5. Solving Poisson's equation in each region of the MODFET yields [49:17]:

$$V_b - V_g = \frac{q N_d d_d^2}{2\epsilon_2} + \Delta E_c - E_{fi} - \frac{q n_s (d_d + d_i)}{\epsilon_1} \qquad (2\text{-}5)$$

where
- n_s = 2DEG carrier concentration
- N_d = Donor concentration in AlGaAs
- d_d = doped AlGaAs thickness
- d_i = undoped AlGaAs thickness
- E_{fi} = potential between Fermi level and bottom of quantum well

When (2-5) is rearranged for n_s

$$n_s = \frac{\epsilon_2}{q(d_d + d_i)} \left[\frac{q N_d d_d^2}{2\epsilon_2} + V_g - V_b + \Delta E_c - E_{fi} \right] \qquad (2\text{-}6)$$

but E_{fi} is also a function of n_s [49:14] and is given by

$$E_{fi} = a n_s + E_{fo} \tag{2-7}$$

where $$a = 1.25 \times 10^{-13} \ V/cm^2 \tag{2-8}$$

$$E_{fo} = 0 \text{ at } 300°K, \ 0.025 V \text{ at } 77°K \tag{2-9}$$

which yields

$$n_s = \frac{\epsilon_2}{q(d_d+d_i)}\left[V_g - V_b + \frac{q N_d d_d^2}{2\epsilon_2} + \Delta E_c - a n_s - E_{fo}\right] \tag{2-10}$$

Rearranging terms, we obtain

$$q\left(d_i + d_d + \frac{\epsilon_2 a}{q}\right) n_s = \epsilon_2 \left[V_g - V_b + \frac{q N_d d_d^2}{2\epsilon_2} + \Delta E_c - E_{fo}\right] \tag{2-11}$$

which leads to the final result

$$n_s = \frac{\epsilon_2}{q(d+\Delta d)}\left[V_g - V_{off}\right] \tag{2-12}$$

where

$$V_{off} \equiv V_b - \frac{q N_d d_d^2}{2\epsilon_2} - \Delta E_c + E_{fo} \tag{2-13}$$

and

$$d = d_i + d_d \tag{2-14}$$

$$\Delta d = \frac{\epsilon_2 a}{q} \approx 80 \text{ Å} \tag{2-15}$$

The added Δd term in the denominator, due to the n_s dependency of E_{fi}, can be thought of as the average depth of the 2DEG in the quantum well. The early charge control models [7,8,9] often overestimated the 2DEG concentration because the n_s dependency of

E_{fi} was not accounted for. The addition of the p+ layer in the ESMODFET will also add a correction factor in the denominator which must be accounted for.

Enhanced Schottky MODFET. The solution of Poisson's equation in each region of the ESMODFET will also yield a result for n_s (see Appendix B). The conduction band diagram obtained by solving Poisson's equation for the ESMODFET is given in Fig 2-11.

Solving Poisson's equation yields (See Appendix B):

$$V_b - V_g = \frac{qN_d d_d^2}{2\epsilon_2} - \frac{qn_s}{\epsilon_2}\left[d_i + d_d + \frac{\epsilon_2 t}{\epsilon_1}\right] - E_{Fi} - \frac{qN_a t^2}{2\epsilon_1} + \frac{qN_d d_d t}{\epsilon_1} \qquad (2\text{-}16)$$

Solving for n_s, and accounting for the n_s dependency of E_{fi} yields the final result

$$n_s = \frac{\epsilon_2}{q(d' + \Delta d)}\left[V_g - V'_{off}\right] \qquad (2\text{-}17)$$

where

$$V'_{off} \equiv V_b + E_{f_o} + \frac{qN_a t^2}{2\epsilon_1} - \frac{qN_d d_d^2}{2\epsilon_2} - \frac{qN_d d_d t}{\epsilon_1} \qquad (2\text{-}18)$$

and

$$d' \equiv d_i + d_d + \frac{\epsilon_2 t}{\epsilon_1} \qquad (2\text{-}19)$$

The result of Eq 2-18 is the same form as found in Eq 2-12, but has the correction in the denominator for the p+ layer. The reason that the p+ GaAs thickness (t) is modified, rather than being added directly, is due to the boundary conditions at the

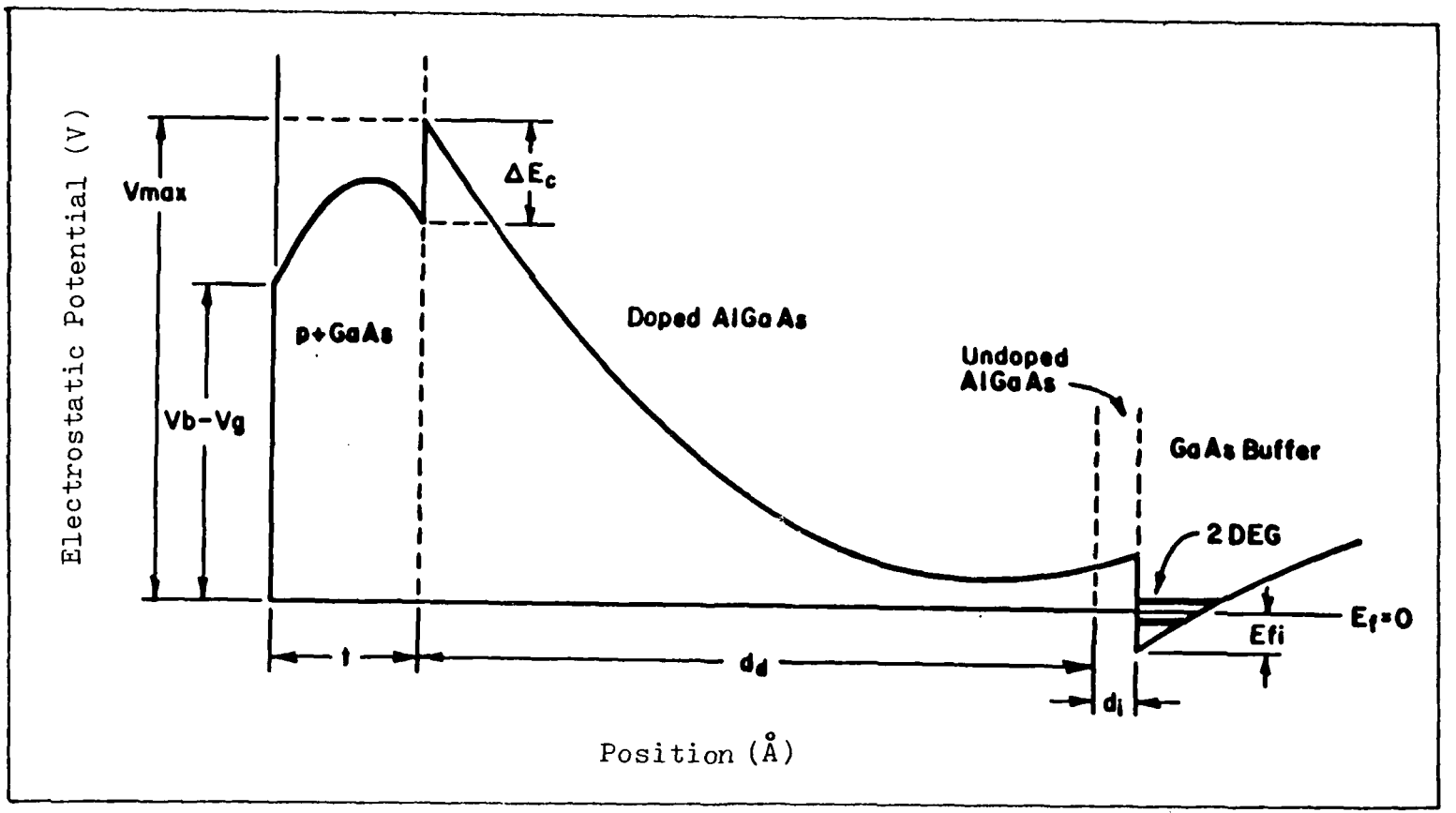


Fig 2-11 Conduction Band Diagram for ESMODFET

heterointerface between the p+ GaAs layer and the AlGaAs layer.

The charge control model can be extended to predict the current-voltage (I-V) characteristics for both the MODFET and the ESMODFET. Thus the real power of the charge control model lies in the relationships between device parameters and the material parameters such as thickness and doping.

Current Control. The application of a voltage between the source and drain (V_{ds}) with $V_g > V_{off}$ will produce a current in the MODFET (I_{ds}). Fig 2-12 depicts the effect of V_{ds} on the channel voltage ($V_c(x)$) as a function of distance, where L is the length of the channel. The effective voltage controlling the charge at a distance x along the channel is given by [49]

$$V_{eff} = V_g - V_c(x) \tag{2-20}$$

where Vg is the applied gate voltage and $V_c(x)$ is the channel voltage as a function of position.

The charge controlled by the gate voltage as a function of position along the channel is simply:

$$Q(x) = \frac{\epsilon_2}{(d+\Delta d)}\left[V_{eff} - V_{off}\right] \tag{2-21}$$

The development of the models used to evaluate the MODFET are based upon the relation [49:19]:

$$I(x) = Q(x) Z v(x) \tag{2-22}$$

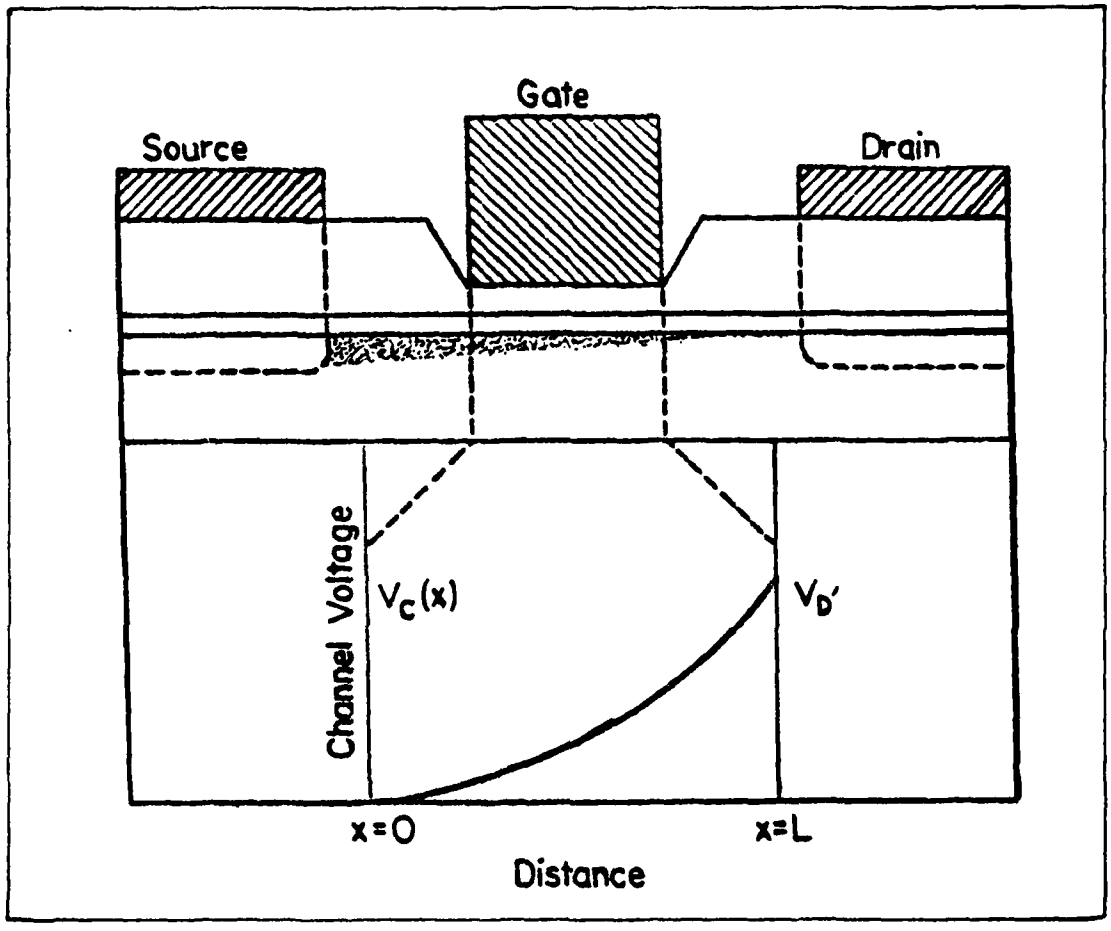


Fig 2-12 Channel Voltage vs Distance for MODFET

where Z = Gate width

$v(x)$ = average velocity of electron at x.

The linear relationship of Eq 2-22 is very good for low values of electric field, but for the short channel lengths of the MODFET, the electric field is fairly large which causes saturation of the electron velocity [5,42,49]. The velocity saturation effect can be modeled with the current increasing linearly with electron velocity until the velocity saturation point ($E = E_s$) is reached. For values of electric field above the saturation point ($E \geq E_s$), the current is constant due to the velocity saturation of the electrons (see Fig 2-13).

The two-piece model of the MODFET is based upon the assumption that the electron reaches its saturation velocity at the drain side of the channel ($x = L$) (see Fig 2-12). The electron velocity increases linearly with increasing electric field for $E < E_s$ and is constant for $E \geq E_s$ according to the relations

$$v = \mu E \quad (E < E_s) \tag{2-23}$$

$$v = v_s \quad (E \geq E_s) \tag{2-24}$$

where

v = electron velocity

μ = low-field mobility of intrinsic GaAs

E = electric field

E_s = electric field at velocity saturation

v_s = saturation velocity

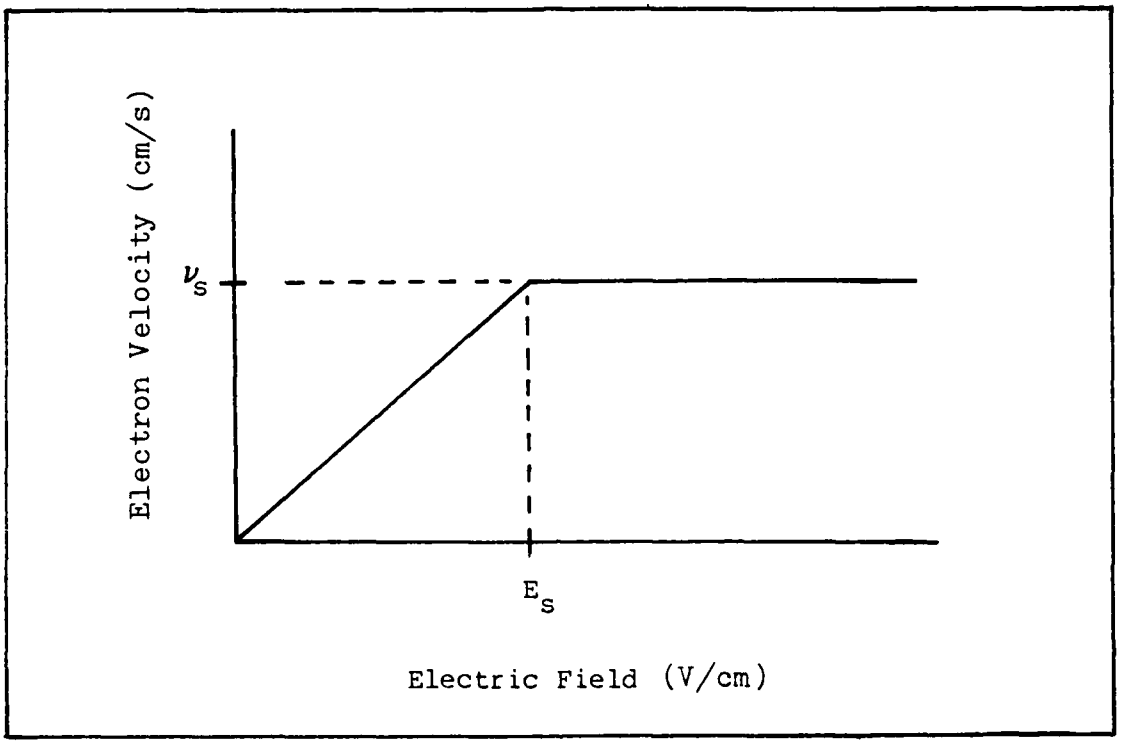


Fig 2-13 Two-Piece Model of Electron Velocity vs Electric Field [49].

which then leads to the expressions [35:209]

$$V_{sat} = V_g' + V_{s1} - \left(V_g'^2 + V_{s1}^2\right)^{1/2} + I_{sat}\left(R_s + R_d\right) \qquad (2\text{-}25)$$

and

$$I_{sat} = \frac{KV_{s1}^2\left[\left(1 + 2KR_sV_g' + \left(\frac{V_g'}{V_{s1}}\right)^2\right)^{1/2} - \left(1 + KR_sV_g'\right)\right]}{\left(1 - K^2R_s^2V_{s1}^2\right)} \qquad (2\text{-}26)$$

where

$$V_g' = V_g - V_{off} \tag{2-27}$$

$$V_{s1} = E_s L \tag{2-28}$$

$$K = \frac{\epsilon_2 \mu Z}{L(d+\Delta d)} \tag{2-29}$$

In these expressions, V_{sat} is the saturation voltage, I_{sat} is the saturation current, L is gate length, and Z is the gate width.

The two-piece model allows for a reasonable prediction of the I-V characteristics of the MODFET. The model can be applied to the ESMODFET by simply replacing d with d' in Eq 2-29. The saturation voltage and current for the ESMODFET are also given by Eqs 2-25 and 2-26 respectively with an alteration in the constant K as given by

$$K = \frac{\epsilon_2 \mu Z}{L(d'+\Delta d)} \tag{2-30}$$

The charge control model can be used to predict the transconductance, capacitance and current characteristics of the MODFET and ESMODFET. The maximum transconductance of the MODFET can be found by differentiating the saturation current with respect to gate voltage [49:23].

Transconductance

The charge control model is easily extended to predict the transconductance of the MODFET. The transconductance is simply the increase in current for a given increase in gate voltage. The

maximum transconductance for the MODFET has been found to be [49:23]

$$g'_m = \frac{\varepsilon\mu Z n_s}{L}\left[1 + \left(\frac{\varepsilon\mu n_s (d+\Delta d)}{\epsilon_2 v_s L}\right)^2\right]^{-1/2} \qquad (2\text{-}31)$$

which for short gate lengths reduces to

$$g'_m = \frac{\epsilon_2 Z v_s}{(d+\Delta d)} \qquad (2\text{-}32)$$

The transconductance for the ESMODFET is found by substituting d' for d in Eqs 2-31 and 2-32. Thus for the ESMODFET

$$g'_m = \frac{\varepsilon\mu Z n_s}{L}\left[1 + \left(\frac{\varepsilon\mu n_s (d'+\Delta d)}{\epsilon_2 v_s L}\right)^2\right]^{-1/2} \qquad (2\text{-}33)$$

which for short gate lengths reduces to

$$g'_m = \frac{\epsilon_2 Z v_s}{(d'+\Delta d)} \qquad (2\text{-}34)$$

The current control model can also be used to find the total charge under the gate of the MODFET, leading to the calculation of the capacitance of the MODFET versus applied gate voltage.

Small Signal Gate Capacitance

The small signal gate capacitance of the MODFET has been calculated using the two-piece model [35,49]. The total charge under the gate for small electric fields is given by [49:24-25]:

$$Q_T = Z\int_0^L \varepsilon n_s \, dx \qquad (2\text{-}35)$$

$$Q_T = Z \int_{V_s}^{V_d} q\, n_s \left(\frac{dx}{dV}\right) dV \qquad (2\text{-}36)$$

Integrating Eq 2-36 yields [49]

$$Q_T = \frac{2C_o\left(V_{gs}^3 - V_{gd}^3\right)}{3\left(V_{gs}^2 - V_{gd}^2\right)} \qquad (2\text{-}37)$$

where

$$C_o = \frac{\epsilon_2 Z L}{(d+\Delta d)} \qquad (2\text{-}38)$$

Differentiating Q_T with respect to V_{gs} yields the gate-to-source capacitance (Cgs)

$$C_{gs} = \frac{2C_o\left(V_{gs} + 2V_{gd}\right)}{3\left(V_{gs} + V_{gd}\right)^2} \qquad (2\text{-}39)$$

Differentiating Q_T with respect to V_{gd} yields

$$C_{gd} = \frac{2C_o\left(V_{gd} + 2V_{gs}\right)}{3\left(V_{gs} + V_{gd}\right)^2} \qquad (2\text{-}40)$$

The capacitances of the ESMODFET are found by replacing d with d' in Eq 2-38. Replacing d with d' yields

$$C_{gs} = \frac{2C_o'\left(V_{gs} + 2V_{gd}\right)}{3\left(V_{gs} + V_{gd}\right)^2} \qquad (2\text{-}41)$$

$$C_{gd} = \frac{2C_o'\left(V_{gd} + 2V_{gs}\right)}{3\left(V_{gs} + V_{gd}\right)^2} \qquad (2\text{-}42)$$

where

$$C_o' = \frac{\epsilon_2 Z L}{(d' + \Delta d)} \qquad (2\text{-}43)$$

The normalized gate-to-drain (C_{gd}) and gate-to-source (C_{gs}) capacitances versus V_{ds} for values of Vg'/V_{sl} for the MODFET are shown in Figs 2-14 and 2-15 respectively [35, 49]. As can be seen both Cgd and Cgs can as large as one-half of the gate capacitance.

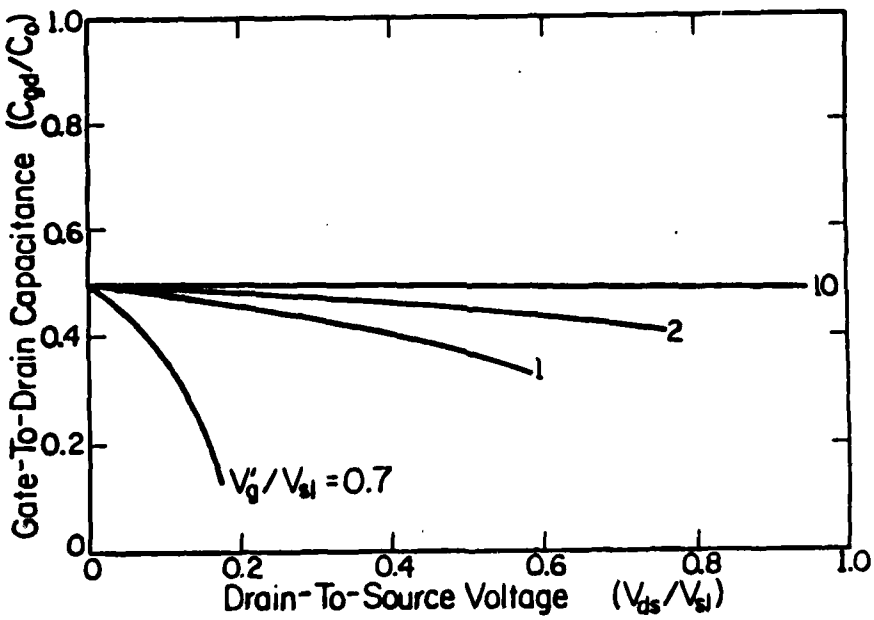


Fig 2-14 Gate-to-Drain Capacitance vs Drain Voltage for Various Values of Normalized Gate Voltage [49].

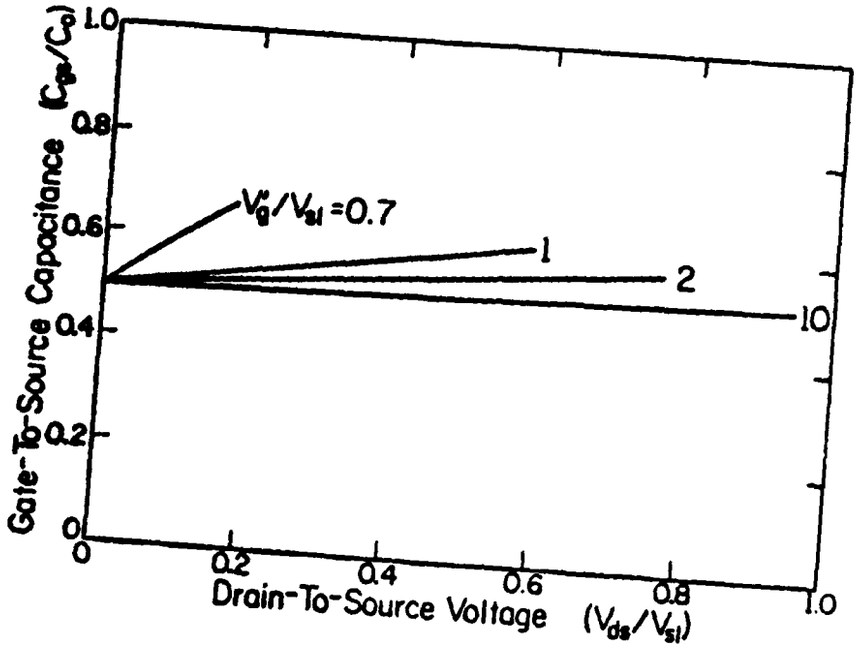


Fig 2-15 Gate-to-Source Capacitance vs Drain Voltage for Various Values of Normalized Gate Voltage [49].

The relationships between the physical characteristics and the electrical characteristics of the MODFET or ESMODFET can be used to determine the layer thicknesses and dopings required for a desired enhanced Schottky barrier (V_{max}) and threshold voltage (V_{off}).

III. Equipment

Fabrication Equipment

The equipment used to test and fabricate the devices in this thesis can be found in any microelectronics facility. The devices were fabricated at the University of Illinois-Urbana and tested at the Avionics Lab, Wright-Patterson AFB, Ohio. The wafers were fabricated by MBE and then processed using spinners, ovens, mask aligners and an evaporation chamber. The fabrication process is explained in detail in Appendix C.

Spinner. The spinner used was manufactured by Headway Research Inc.. The important features required for the spinner are a vacuum chuck to hold the wafer in place and the capability to spin the wafer at 5000 rpm. The wafers were spun at 5000 rpm for 30 seconds after the photoresist was applied.

Mask Aligner. The mask aligner used to expose the photoresist was a Karl Suiss model MTB 3HP UV400. The intensity used to expose the photoresist was 8.7 mW/cm^2. The samples were all exposed for six seconds. The aligner used for fabrication must be able to handle device geometries with 1 μm gate lengths.

Prebake Ovens. The ovens used for pre-bake, softbake, and drying the wafers were metal boxes with the temperature controlled by hotplates. Each hot plate had controls which could be adjusted to keep the ovens at a constant temperature. The ovens were operated at either 90°C or 110°C.

Alloying Oven. The alloying oven used was heated to 500°C. Nitrogen was used to purge the oven before samples were placed in the oven. The oven was the purged with nitrogen for three minutes after the wafers were placed within the tube. After purging, the wafers were pushed into the oven for 50 seconds. After the 50 second alloying bake, the wafers were again kept in the tube for three minutes while the oven was purged. The wafers were then removed from the tube.

Evaporation Chamber. The evaporation chamber was a standard bell-type chamber made by Perkin-Elmer with a Sloan PAK 8 electron gun used to bombard the target. The evaporation process involved mounting the wafer samples, placing the the metal pellets to be deposited in the appropriate crucibles, checking the seal, and then the chamber was evacuated to below 10^{-6} torr. After the proper pressure was reached, the metal sources were evaporated in sequence automatically. The gate metal for the devices used in this thesis were made by depositing a layer of Ti and then a thin layer of Au. The source and drain contacts were formed by depositing a AuGe alloy, Ni, and then Au in sequence. One series of samples had an Al gate metal deposited, but they did not operate properly when fabricated. After the metal evaporation step was completed, the wafers were removed and the excess metal was lifted off as outlined in Appendix C.

Test Equipment

The test equipment used to determine the dc characteristics of the ESMODFETs consisted of a current source, a digital multimeter, and a semiconductor parameter analyzer.

Current Source. A Hewlett-Packard model 6181B dc current source was used as the current source for the source resistance measurement for the ESMODFET. The HP 6181B had a low current range which was used to make the resistance measurement without passing too much current through the devices.

Digital Multimeter. A HP model 3465b digital multimeter was used for the source resistance measurements. The multimeter had a current meter, voltmeter, and resistance meter capability. The current meter was used to record the current output by the current source, while the voltmeter was used to measure the voltage from drain to source for a given current.

Semiconductor Parameter Analyzer. The HP 4145A Semiconductor parameter analyzer was used to determine many of the dc characteristics of the ESMODFET. A picture of the analyzer is given in Fig 3-1. The analyzer has the capability of computer control, but this feature was not utilized during testing. The analyzer can be quickly switched from measuring one set of parameters to measuring another without changing the probes. The desired settings for V_{ds}, V_g, I_{ds} could be stored in user files for each test set-up and called up at will. The capabiltiy for storing preset values for voltages and measurement set-ups, gives the analyzer a big advantage over the standard curve tracer. The

analyzer is nothing more than a computerized curve tracer. The screen can be photographed, or the data can be reproduced with a plotter as shown in Appendix D.

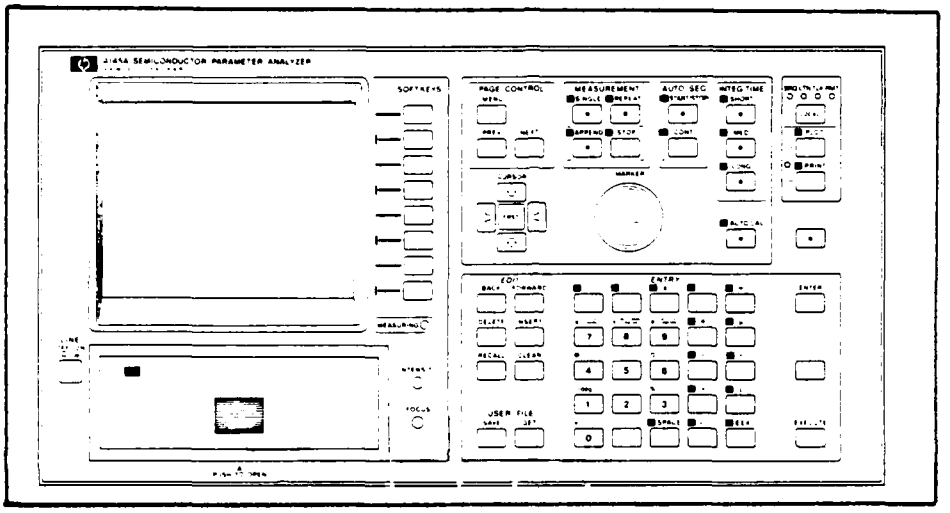


Fig 3-1. HP 4145 Semiconductor Analyzer

The fabrication and testing of the devices was done after the appropriate doping and thickness for each semiconductor layer was determined for a desired threshold voltage (V_{off}) and enhanced Schottky barrier (V_{max}). The theory used to determine the required thickness and doping for each layer is developed in Chapter 4.

IV Experimental Design

The fabricaton of the ESMODFET is a two-step process. The first step is to determine the layer thicknesses necessary for the desired barrier height (V_{max}) and turn-on voltage (V_{off}). The second step involves fabricating the devices. This chapter will develop the theory used to design the ESMODFET and the procedure used in fabrication.

Layer Thickness Design

The theory developed in chapter 2 can now be used to predict the required layer thicknesses of the ESMODFET. The layer design must be divided into two cases, enhancement devices ($V_{off}>0$) and depletion devices ($V_{off}<0$). The theory used to obtain the required layer thicknesses is slightly different for each case.

Enhancement Devices ($V_{off}>0$). The layer thicknesses required to fabricate an enhancement device can be determined from Eq B-49 which is derived in Appendix B.

$$V_{off} \equiv V_b + \frac{qN_a t^2}{2\epsilon_2} - \frac{qN_d d_d t}{\epsilon_1} - \frac{qN_d d_d^2}{2\epsilon_2} + E_{F_0} \qquad \text{(B-49)}$$

Where V_b = metal-p+ Schottky barrier

N_a = p+ GaAs layer doping

t = p+ GaAs layer thickness

N_d = AlGaAs layer doping

d_d = AlGaAs layer thickness

ϵ_1 = permittivity of GaAs

ϵ_2 = permittivity of AlGaAs

E_{Fo} = 0V @ 300K, .025V @ 77K.

Adding and subtracting the conduction band discontinuity ΔE_c for each heterojunction and rearranging terms yields

$$V_b = \Delta E_c + V'_{OFF} + \frac{qN_d d_d^2}{2\epsilon_2} + \frac{qN_d d_d t}{\epsilon_1} - \frac{qN_a t^2}{2\epsilon_1} - \Delta E_c - E_{Fo} \qquad (4\text{-}1)$$

Plotting the associated band diagram for Eq 4-1 will give some insight into the problem as shown in Fig 4-1.

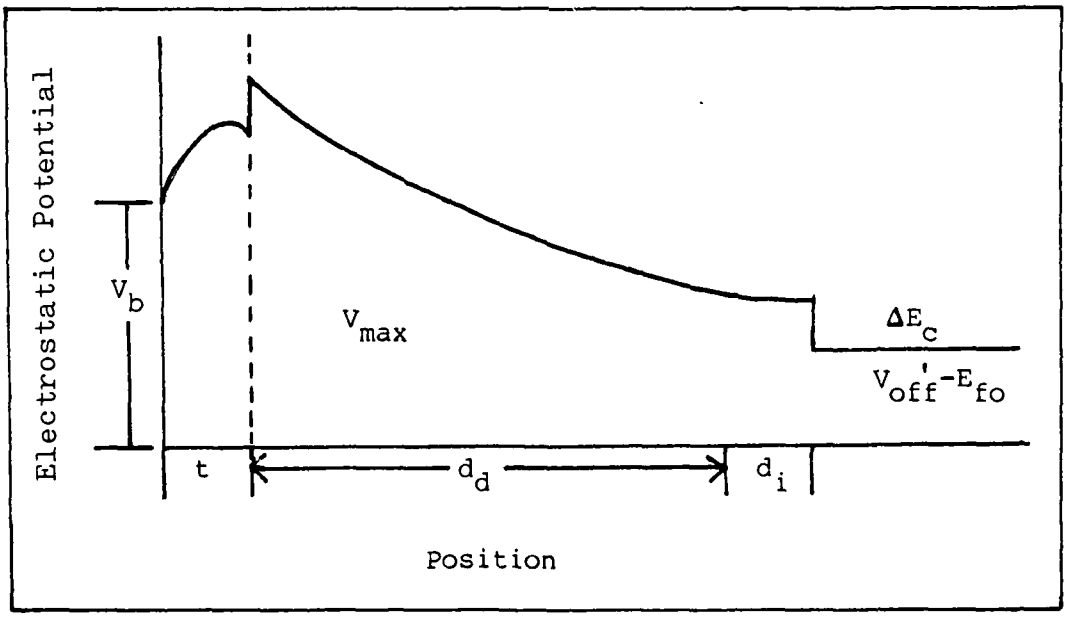


Fig 4-1 Conduction Band Diagram of ESMODFET for $V_{off}>0$.

From Fig 4-1 we obtain

$$V_{max} = V_{OFF}' + \Delta E_c - E_{Fo} + \frac{q N_d d_d^2}{2\epsilon_2} \qquad \left(V_{OFF}' \geq 0\right) \qquad (4\text{-}2)$$

This expression is equivalent to Eq B-43 when $V_{off}=0$

$$V_{max} \equiv \frac{q N_d d_d^2}{2\epsilon_2} - \frac{q n_s d}{\epsilon_2} + \Delta E_c - E_{Fi} \qquad (B\text{-}43)$$

Thus solving Eq 4-2 for d_d yields

$$d_d = \left[\frac{2\epsilon_2}{q N_d}\left(V_{max} - V_{OFF}' + E_{Fo} - \Delta E_c\right)\right]^{1/2} \qquad (4\text{-}3)$$

which is the required AlGaAs layer thickness

Thus the required AlGaAs thickness (d_d) for a given V_{max} and V_{off} has been determined. Now, the required thickness (t) of the p+ GaAs, which will deplete the AlGaAs as well as produce the desired dc offset (V_{off}') at the 2DEG interface, must be determined. Solving Eq (4-1) for t, we find

$$t = \frac{N_d d_d}{N_a}\left[1 + \left(1 + \frac{N_a \epsilon_1}{N_d \epsilon_2} - \frac{2\left(V_b - V_{OFF}' + E_{Fo}\right) N_a \epsilon_1}{q N_d^2 d_d^2}\right)^{1/2}\right] \qquad (4\text{-}4)$$

Thus the required layer thicknesses for the enhancement ESMODFET have been determined. Determining the layer thicknesses of the depletion mode ESMODFET is an extension of the concepts used for the enhancement device. When V_{off}, V_{max}, N_a, N_d, and the

Al mole fraction are known, the required thicknesses can be found. The theory developed in this thesis assumes that all of the dopants are ionized in the AlGaAs and GaAs layers. This assumption is fairly good at 300°K once the effect of compensation is taken into account. The actual results obtained can differ from those predicted by using the flux values of the dopants due to compensation mechanisms in the layers themselves. Once the effective doping has been determined the theory should match the experimental results. For typical n-type AlGaAs layers, the net amount of donors available is typically 65% of the doping concentration [18:162,69] initially incorporated into the sample. Because of the uncertainty of the actual doping concentration, when the device characteristics are measured, only the layer thicknesses, V_{off}, V_{max} and x will be known. The effective doping concentrations for $V_{off} \geq 0$ can be obtained from the expressions given below.

$$N_d = \frac{2\epsilon_2}{q d_d^2}\left(V_{max} - V_{off}' - \Delta E_c\right) \tag{4-5}$$

and

$$N_a = \frac{2\epsilon_1}{q t^2}\left(V_{off}' - V_b - E_{fo} + \frac{q N_d d_d t}{\epsilon_1} + \frac{q N_d d_d^2}{2\epsilon_2}\right) \tag{4-6}$$

Depletion Devices ($V_{off} \leq 0$). The layer thicknesses of depletion mode devices are not quite as simple to calculate as

those of the enhancement devices. The conduction band diagram is now affected by the 2DEG concentration (n_s). The conduction diagram for the depletion device is given in Fig 2-12. The solution to Poisson's equation for the depletion mode ESMODFET given in Eqs 2-15 through 2-18. The maximum barrier (V_{max}) is then given by Eq B-43.

The dependence of V_{max} on n_s requires an iterative process to obtain the desired V_{max}, V_{off}, and n_s. However, the n_s dependency is not critical, so an approximation can be made which eliminates the n_s dependency and still yields very good results. The key to determining d_d is a knowledge of the band diagram when V_{off} = 0. This diagram is given in Fig 4-2.

The maximum is given by Eq 4-1 with Voff=0. The depletion depth (W) required for the AlGaAs layer to give the desired Vmax is determined by Eq 4-3 with W replacing d_d. The thickness of the p+ layer is given by Eq 4-4 with W replacing d_d and setting V_{off} equal to zero. Thus

$$W = \left[\frac{2\epsilon_2}{q N_d}\left(V_{max} - \Delta E_c + V_{OFF}\right)\right]^{1/2} \qquad (4\text{-}7)$$

and

$$t = \frac{N_d W}{N_a}\left[1 + \left(1 + \frac{N_a \epsilon_1}{N_d \epsilon_2} - \frac{2 V_b N_a \epsilon_1}{q N_d^2 W^2}\right)^{1/2}\right] \qquad (4\text{-}8)$$

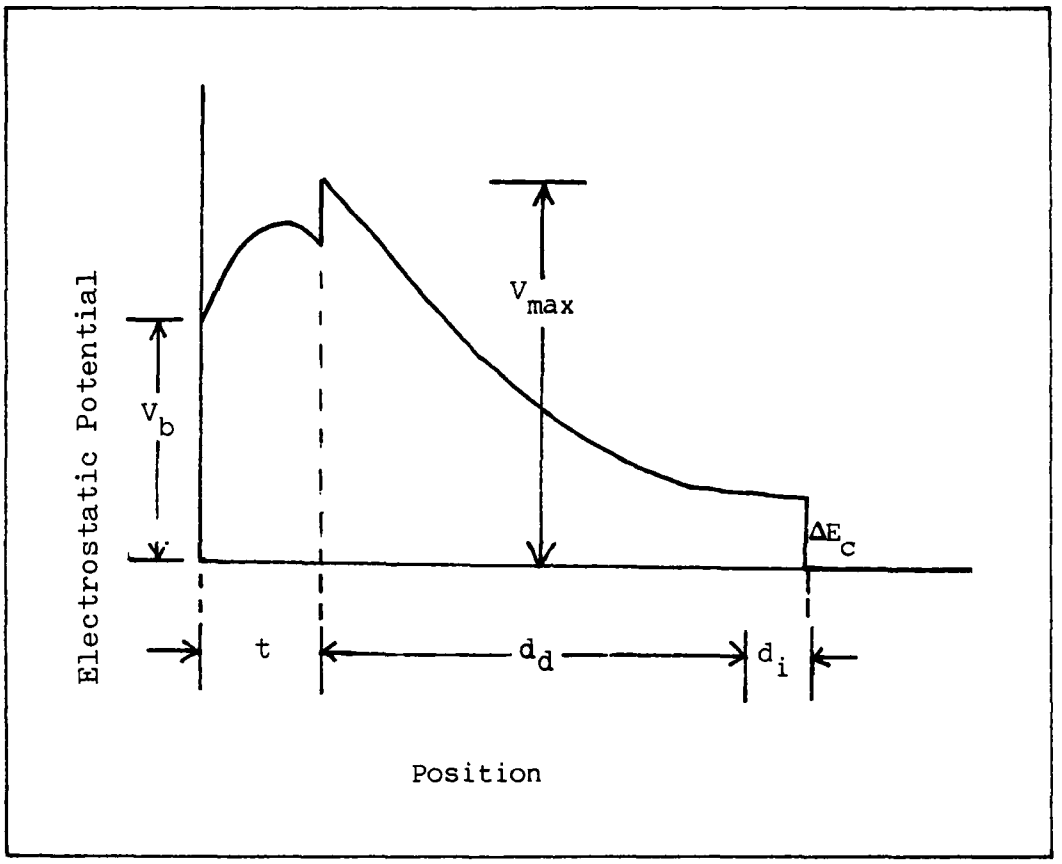


Fig 4-2. ESMODFET Conduction Band Diagram for V_{off}=0.

The addition of doped AlGaAs forces V_{off} to be less than zero with a corresponding 2DEG concentration appearing in the channel. Solving Eq B-49 for d_d yields

$$d_d = \frac{\epsilon_2 t}{\epsilon_1}\left[\left(1 + \frac{\epsilon_1 N_a}{\epsilon_2 N_d} + \frac{2\epsilon_1^2\left(V_b - V_{off}' + E_{Fo}\right)}{q N_d \epsilon_2 t^2}\right)^{1/2} - 1\right] \quad (4\text{-}9)$$

The n_s term combined with E_{fi} in Eq B-43 is approximately the same magnitude as the additional increase in the parabolic term for $d_d > W$. Thus Eq 4-2 is a fairly good approximation for depletion mode devices as well as enhancement devices. To illustrate the fit of the approximation, Fig 4-3 is given. The maximum used to predict the layer thicknesses is $V_{max} = 1.2V$. As can be seen, the solution of Eq B-43, which is shown as the peak in the figure, is the actual solution for the layer thicknesses and doping concentrations used. V_{max} has a value of 1.16V. This result is fairly close to the original value used to predict the layer thicknesses. As V_{off} approaches zero, the fit is better until it is exact for V_{off} greater than zero.

Thus the layer thicknesses for the ESMODFET can be determined given the desired V_{max}, V_{off}, N_a, and N_d. The first two samples did not have their thicknesses tailored in the manner just described. The samples were grown, and then V_{off} and V_{max} were estimated. Table 4-1 gives the doping, layer thicknesses, predicted barrier heights, and turn-on voltages for the samples fabricated for this thesis.

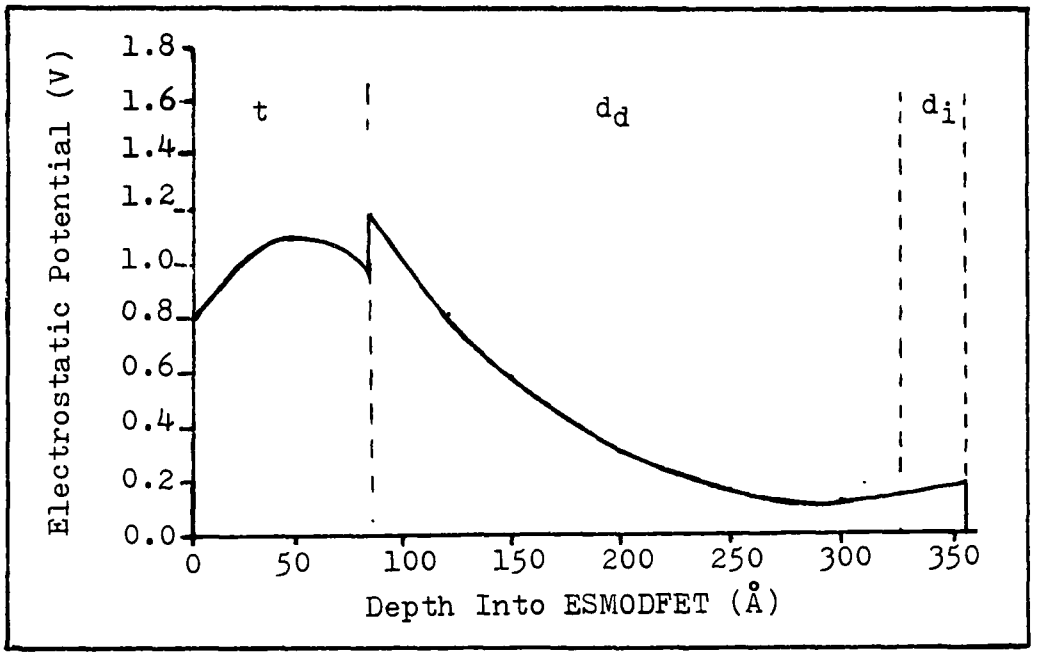


Fig 4-3. Conduction Band Diagram for V_{max} = 1.2, V_{off} = -0.5, Using the Approximation of Eq 4-1

Table 4-1 Samples used in Thesis

Sample	N_a	N_d	t	d_d	d_i	x	V_b(V)	V_{off}(V)	V_{max}(V)
2263	2E19	3E18	100	320	30	0.3	0.8	-1.39	1.38
2265	2E19	3E18	75	350	30	0.3	0.8	-2.19	1.12
2373	2E19	3E18	100	320	30	0.3	0.8	-1.39	1.38
2376	2E19	3E18	75	350	30	0.3	0.8	-2.19	1.12
2377	2E19	3E18	75	320	30	0.3	0.8	-1.66	1.04
2378	2E19	3E18	100	350	30	0.3	0.8	-1.96	1.29

E18 = 10^{18} cm^{-3}, E19 = 10^{19} cm^{-3}; t, d_d, and d_i are in Å

Device Fabrication

The fabrication procedure used in this thesis is given in Appendix C. This section will discuss in general terms the method used to fabricate the devices. Fig 4-4 shows the steps used in the fabrication procedure.

The procedure used is the standard MODFET procedure used at the University of Illinois, with the exception of the last step. The removal of the p+ layer in areas away from the gate (step 6) is necessary to prevent charge in the p+ layer from depleting the 2DEG in the regions away from the gate, thus insuring that the 2DEG will be present in the regions away from the gate. some of the samples had the gate placed directly on the AlGaAs layer. The metal was placed on the AlGaAs by etching the p+ layer through the gate mask, applying the gate metal, and then etching away the remainder of the p+ layer as done in step 6.

After the devices were fabricated, they were inspected for defects and then tested. The tests include measuring the transconductance, the Schottky barrier, the turn-on voltage, the contact resistance, parasitic reistances, and the drain I-V characteristics.

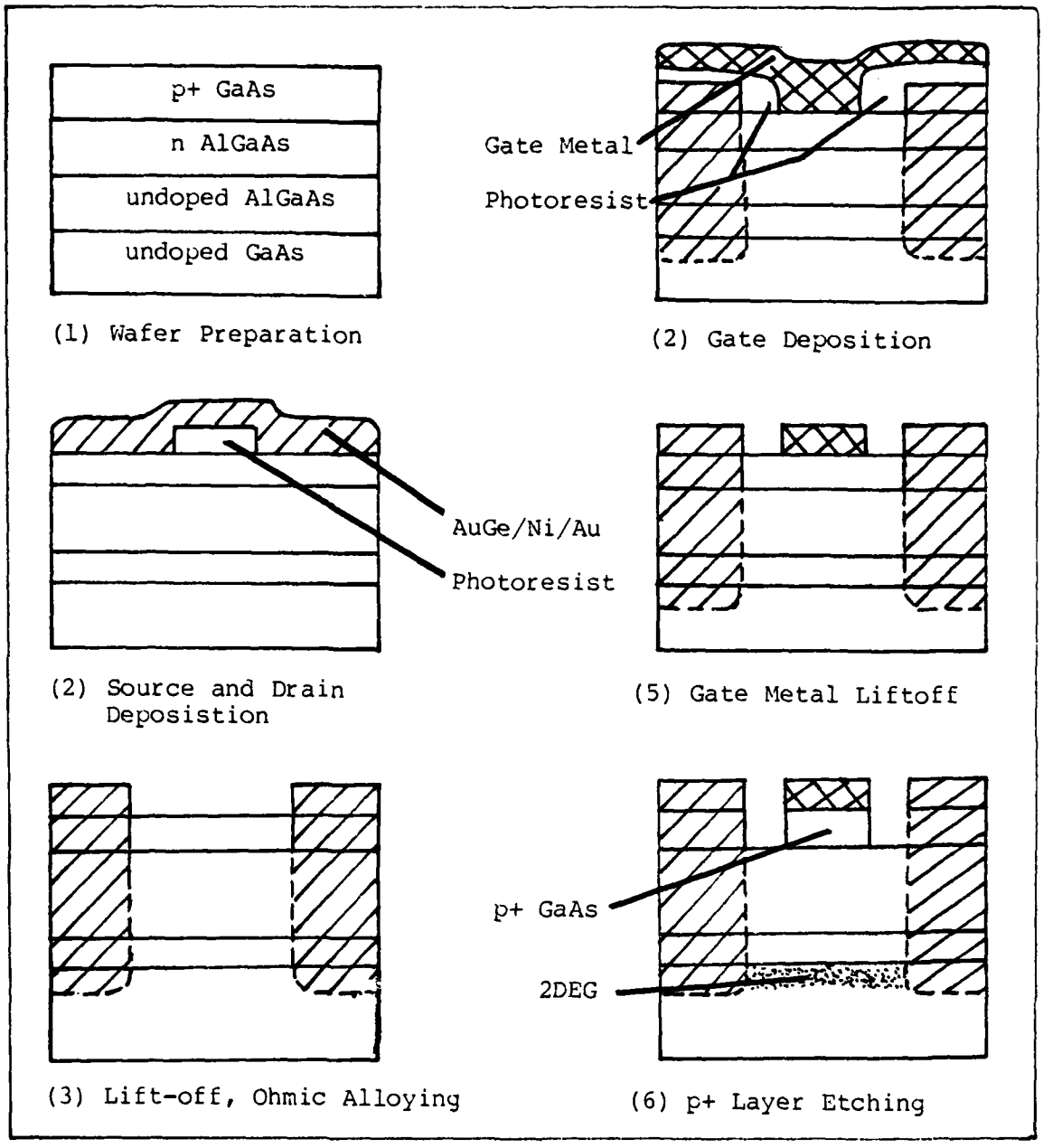


Fig 4-4. Fabrication Process for ESMODFET

V Experimental Results

The experimental results obtained for the ESMODFETs were dc measurements of their perfromance characteristics. No attempt was made to test the microwave performance of the devices. The measurements include the modified Schottky barrier height (V_{max}), the transconductance (g_m), the turn-on voltage V_{off}, the various resistances for the source, drain and gate, contact resistance (R_c), and the normal drain I-V curve for the FET. Representative characteristics for each sample are included in Appendix D.

Schottky Barrier Modification

The devices fabricated for this thesis exhibited a noticeable increase in Schottky barrier height. The barrier height was measured using the gate I-V curve as shown in Fig 5-1. Normal MODFETs have a Schottky barrier of 0.8eV versus a barrier height between (0.8-1.60)eV for ESMODFETs. The actual increase in barrier height was determined by fabricating MODFETs from the same wafer as the ESMODFETs. Control samples were fabricated by etching away the p+ layer and placing the gate contact directly on the AlGaAs on one piece of substrate, while another piece of the same substrate was used for the ESMODFET.

The intersection of the extrapolated lines shown in Fig 5-1 with the x axis was recorded as the Schottky barrier height. The results for V_{max} and V_{off} are given in Table 5-1.

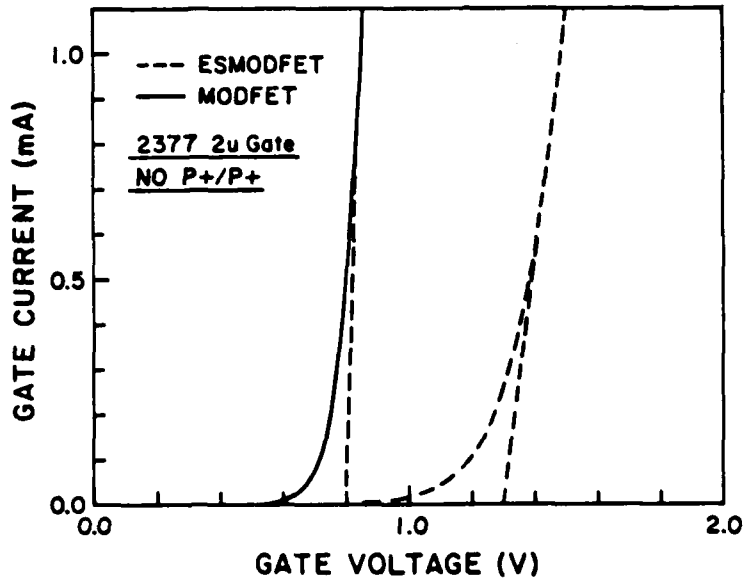


Fig 5-1 Gate I-V Curve for MODFET and ESMODFET Fabricated from Sample 2377.

Turn-on Voltage

The turn-on voltage (V_{off}) was measured by plotting the square-root of I_d versus V_g (see Fig 5-2) and then extrapolating the linear portion of the curve near $I_d = 0$ down to the V_g axis. The intercept was then recorded as V_{off}. Another method of measuring would be to extropolate the transconductance curve when it starts to rise above zero (see Fig 5-3) back to the V_g axis. As can be seen, the two measurement techniques give similar results.

The results obtained for V_{off} and V_{max} were then used to predict the effective p+ and AlGaAs concentrations as shown in chapter 6.

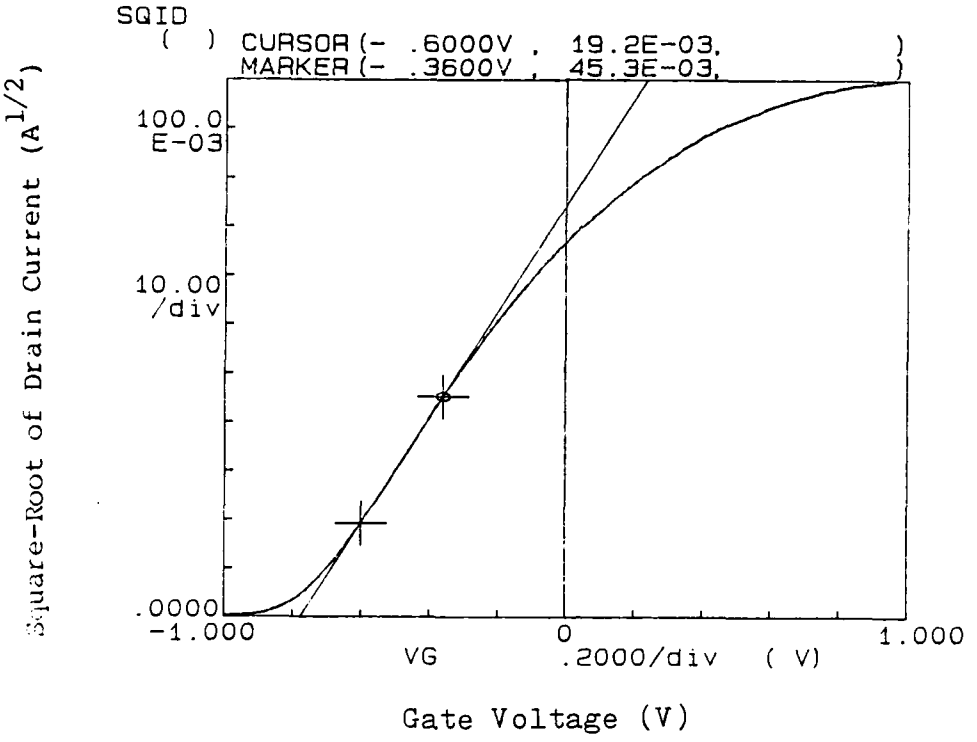


Fig 5-2 I-V Curve used to Determine V_{off} for Sample 2377.

Table 5-1 Turn-on and Schottky Barrier Measurements for ESMODFET Samples.

Sample	V_{off}	V_{max}
2263-1A	0.167	1.14
2265-1A	-0.20	1.07
2373-1A	-0.72	1.30/1.58*
2376-1A	-0.95	1.15
2377-1A	-0.74	1.32/1.55*
2378-1A	-1.15	1.55

* These samples had several devices with V_{max} at each value.

Transconductance

The transconductance of the MODFET and ESMODFET is determined by measuring the change in drain current divided by the change in gate voltage. The result is plotted versus gate voltage (Fig 5-3) while accounting for the gate length of 100 μm. Thus the transconductance (g_m) is given by

$$g_m = \frac{\Delta I_d}{\Delta V_g Z} \quad (mS/mm) \qquad (5\text{-}1)$$

The results are recorded in Table 5-2. The transconductance measured is the extrinsic transconductance. To compare the actual transconductance (g_m) to the maximum (g_m') the following relationship must be used [75:376].

$$g_m' = \frac{g_m}{(1 - g_m Z R_s)} \quad (mS/mm) \qquad (5\text{-}2)$$

where R_s = Source resistance

g_m' = Intrinsic Transconductance

g_m = Measured Transconductance

Resistance Measurements

The resistances of the ESMODFET are measured using standard techniques. The source resistance is measured using the technique shown in Fig 5-4. Because of the high input impedance of the voltmeter, very little current flows through the drain resistance

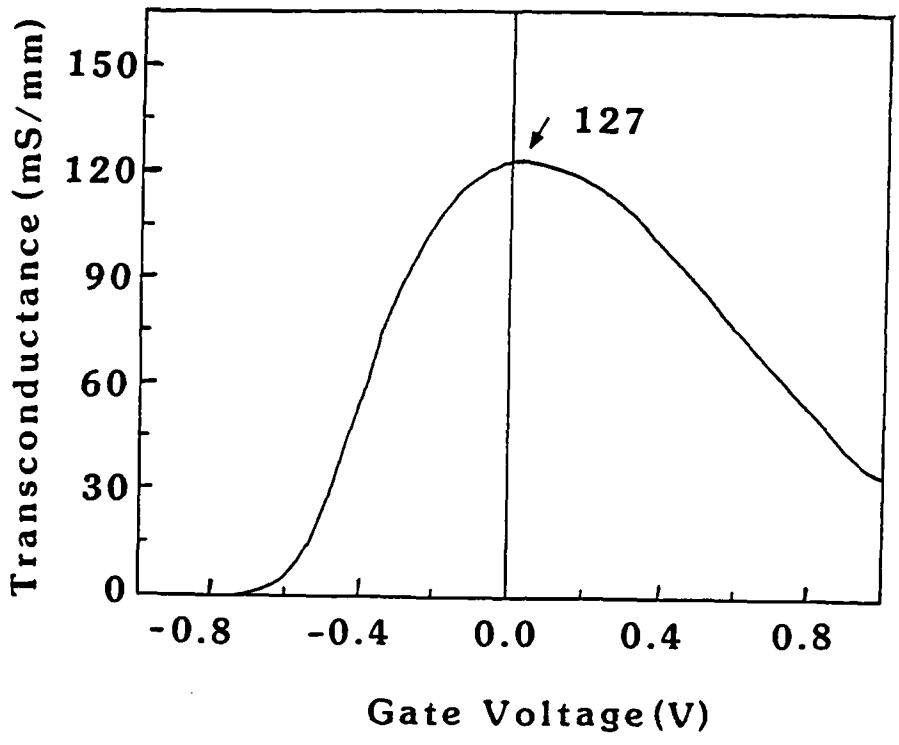


Fig 5-3. Transconductance vs Gate Voltage for Sample 2377.

Table 5-2 Transconductance of ESMODFET Samples

Sample	g_m (mS/mm)	g_m' (mS/mm)
2263-1A	83	122.6
2265-1A	71	102.5
2273-1A	105	142.6
2376-1A	130	239.7
2377-1A	125	205.4
2378-1A	75	122.6

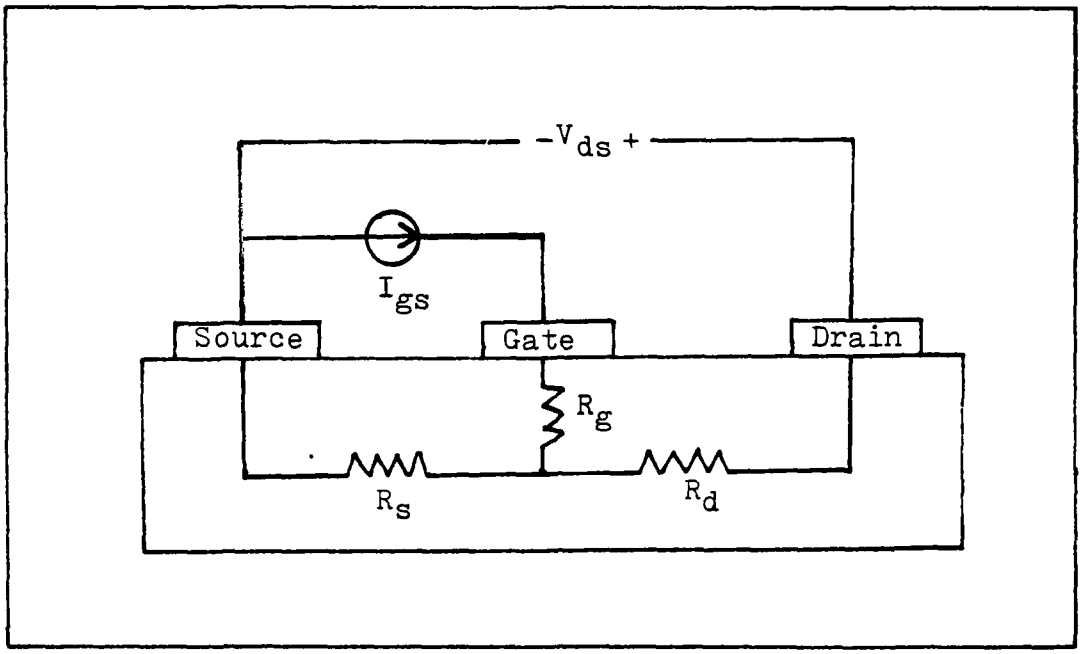


Fig 5-4 Circuit Diagram for Source Resistance Measurement.

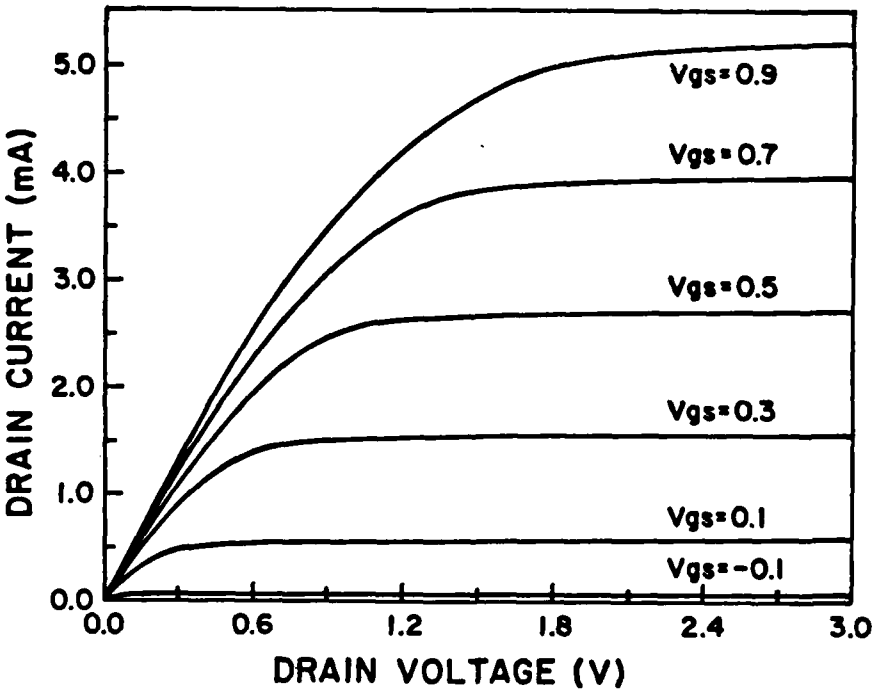


Fig 5-5 Drain I-V Characteristics of ESMODFET from Sample 2265.

which translates into all of V_{ds} being dropped across R_s. Thus by Ohm's law, R_s can be determined. The inverse slope of the FET I-V curve shown in Fig 5-5 is the combined drain and source resistance (R_{sd}). Thus, the drain resistance (R_d) is obtained by subtracting R_s from R_{sd}. The inverse slope of the gate I-V curve (see Fig 5-1) can be used to find the combined source and gate resistance (R_{sg}). The gate resistance (R_g) is found by subtracting R_s from R_{sg}. Care must be taken when using the gate I-V curve, because the probe resistance is also included, whereas in the case of Fig 5-6 the probe resistance has virtually no effect on the measured result of R_{sg} because it is much smaller than the input impedance of the voltmeter. The results of the resistance measurements are given for several devices in Table 5-3.

Table 5-3 Resistance Values for ESMODFETs

Sample	R_s (Ω)	R_{sg} (Ω)	R_g (Ω)	R_{sd} (Ω)
2263-1A	38.9	80.9	42.0	117.9
2265-1A	43.3	77.1	33.8	176.6
2373-1A	25.1	110.0	84.9	93.8
2376-1A	35.2	144.6	109.4	112.5
2377-1A	31.3	157.0	125.7	92.3
2378-1A	51.8	144.0	92.2	109.4

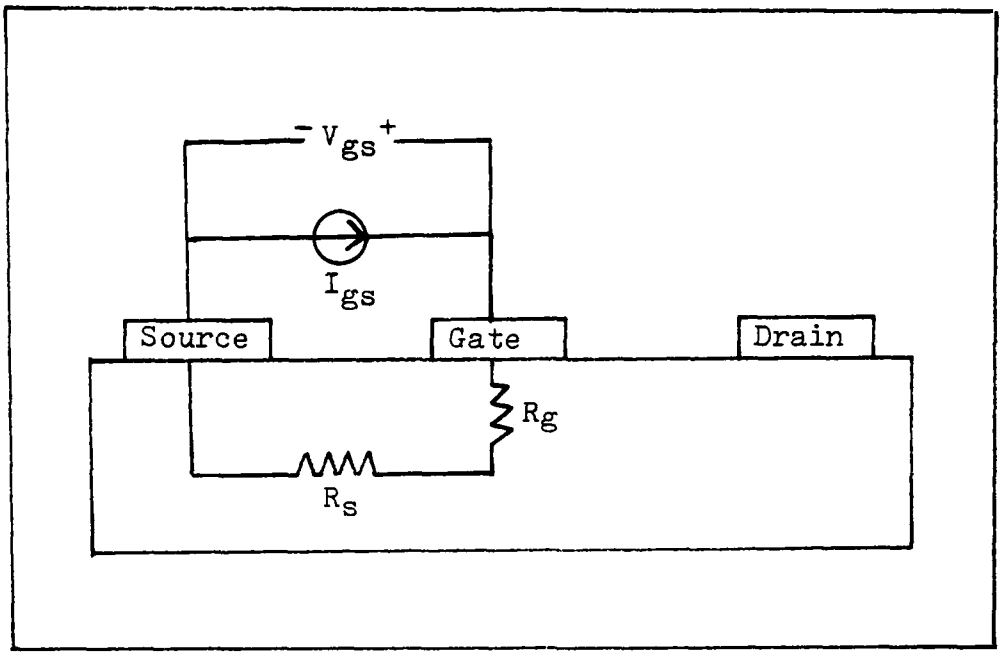


Fig 5-6 Circuit Diagram for Measuring Combined Source and Gate Resistance.

Ohmic Contact Measurement

The ohmic contact measurements were made using the transmission line method (TLM) [75:245]. The TLM involves measuring the resistance between adjacent contact pads in a test pattern which has various distances between adjacent pads. The HP 4145A was used to measure the diode characteristics between the contacts. The probes were adjusted until a linear I-V curve was obtained. The inverse slope of the I-V curve is the resistance between the two contacts. The I-V curve for a pair of contacts is given in Fig 5-7. The resistance of several contact pairs is then plotted for various spacings (L) between pads. A least

squares fit was then made to the data to find the resistance value obtained at the y intercept (L=0). This resistance is equal to to twice the contact resistance (R_c) [75:245-250]. The contact resistance measurements for each sample are given in Table 5-4 with the resulting Rc in ohms and in ohm-mm for a pad length of 75 μm.

The ohmic contact resistances obtained for the ESMODFET samples were between 0.65 Ω-mm and 1.45 Ω-mm, with all but one sample (2373) below 1.0 Ω-mm. These values of contact resistance are very good for room temperature measurements. This result indicates that the p+ layer has little or no effect on the ohmic contact resistance. The ESMODFET contact resistance is in the same range as the normal contact resistance obtained using the n+ capping layer in MODFETs.

The results of this chapter were then evaluated as described in Chapter 6.

Table 5-4 Ohmic Contact Resistance Measurements

Sample	R(5μm)	R(10μm)	R(15μm)	R(20μm)	Fit	Rc (Ω)	Rc (Ω-mm)
2263-1A	30.5	46.2	53.6	71.2	0.98	9.00	0.68
2265-1A	108	290*	308	383	1.00	9.35	0.70
2373-1A	55.9	79.5	97.5	114	0.99	19.33	1.45
2376-1A	39.0	55.9	71.0	89.5	1.00	11.17	0.83
2377-1A	36.4	52.8	67.9	83.5	1.00	10.53	0.79
2378-1A	48.5	72.9	101	118	0.99	12.98	0.97

* data point was invalid due to damaged pad.

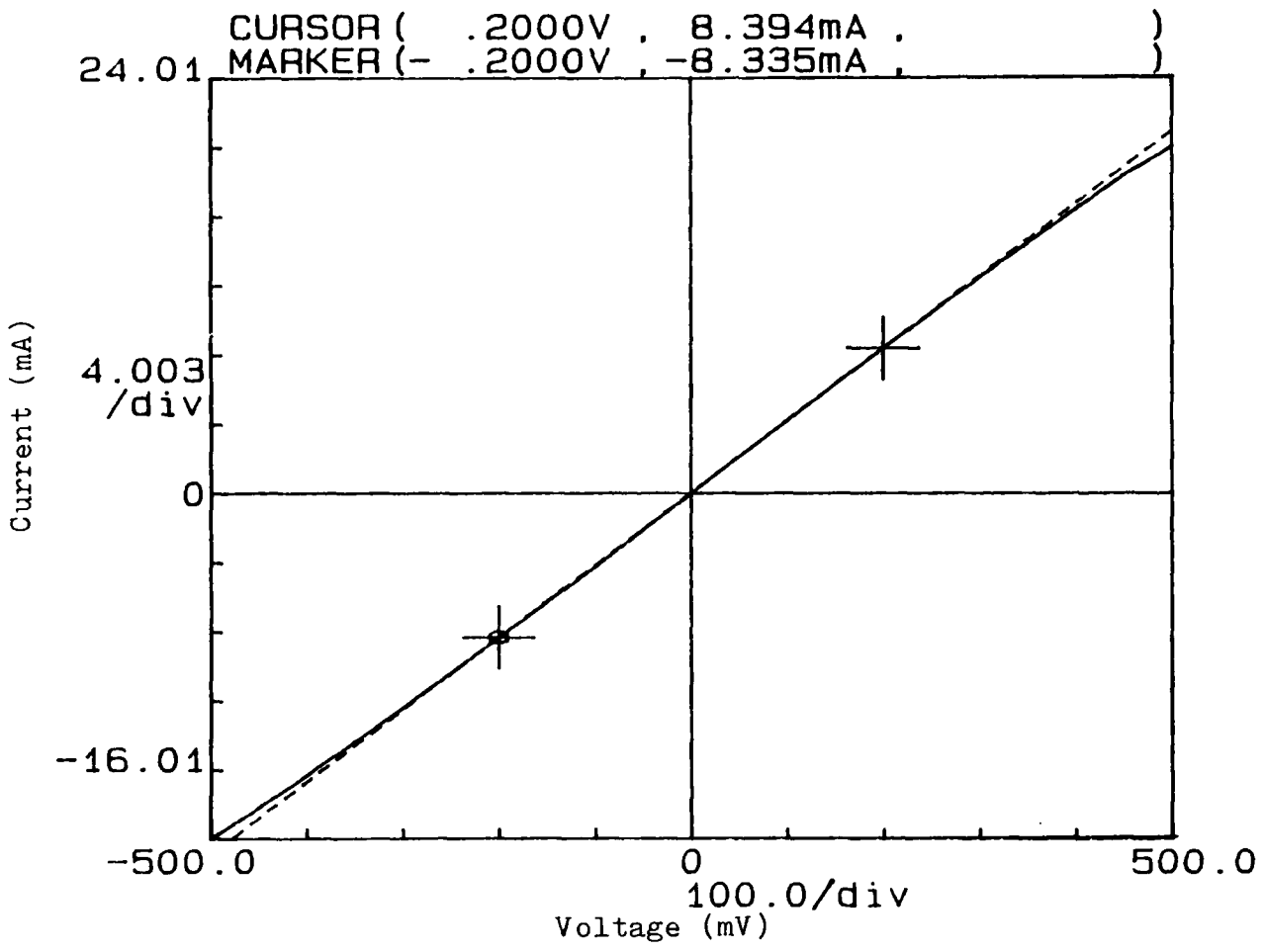


Fig 5-7. I-V Curve for a Pairof Contact Pads

VI Discussion of Results

The results of Chapter 5 show that it is possible to increase the Schottky barrier height of the MODFET. The correlation with theory is much more difficult to show due to the large number of variables which have a determination on the final value of V_{max} and V_{off}, as well as n_s. This chapter will discuss the correlation between theory and experiment for the Schottky barrier, turn-on voltage, and the effective doping concentration of the AlGaAs and GaAs layers. In addition, the fabrication process and its effect on the ESMODFET will also be discussed.

Schottky Barrier Height

The enhanced Schottky barrier height (V_{max}) was very consistent for samples 2263, 2265, and 2378. The other three samples (2373,2376,2377) had barrier heights which varied across the wafer and from device to device. The various measured barriers are given in Table 6-1 with V_{max1} representing the mean value of the barrier most frequently measured, and V_{max2} representing the mean value of the other barrier which was also observed several times. The results appear bimodal in nature for samples 2373, 2376, and 2377. An example of the two barrier measurements is given in Fig 6-1. These measurements were made with the gate I-V curves as described in chapter 5.

Table 6-1 Measured Schottky Barriers Using Gate I-V

Sample	V_{max1} (V)	V_{max2} (V)
2263	1.16	----
2265	1.06	----
2373	1.32	1.56
2376	1.60	1.42
2377	1.53	1.35
2378	1.44	----

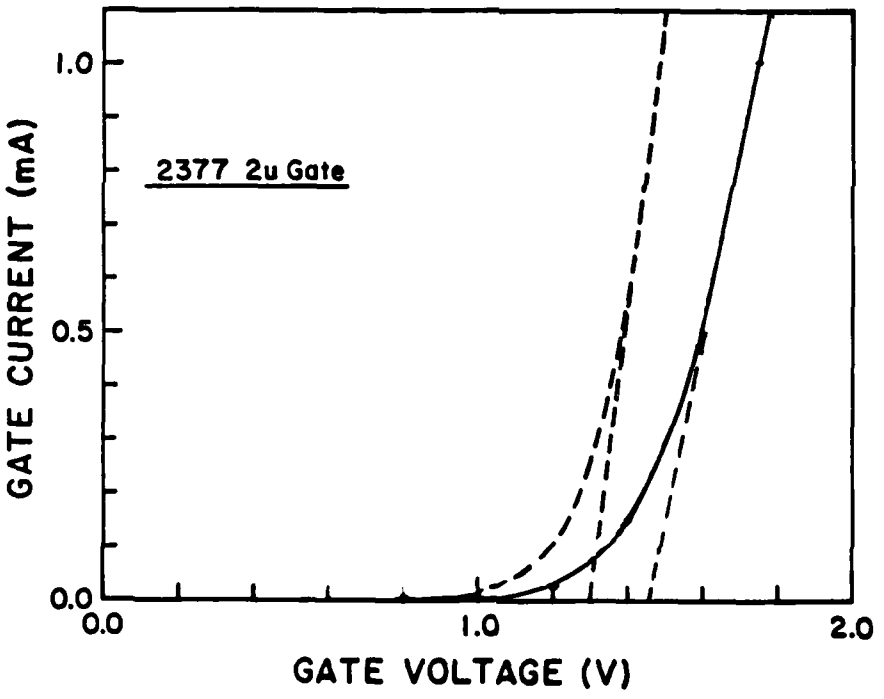


Fig 6-1. Gate I-V for Two 2 μm Devices on Sample 2377.

The variation in the measured Schottky barriers could be due to several factors such as 1) lattice strain, 2) localized differences in doping, 3) mole fraction variation, 4) an oxide layer under the gate metallization, or 5) a rectifying probe contact at the gate when measuring.

The lattice strain and mole fraction variation will effect the conduction band discontinuity (ΔE_c) [3,19,38], increasing or decreasing the Schottky barrier as ΔE_c increases or decreases. Although the mole fraction or lattice strain could explain the differences, it is doubtful that the magnitude of the difference would be as great as that observed.

The effect of varying the doping concentrations and calculating V_{max} and V_{off} can be quite dramatic. If the doping is off by only 10 to 15 percent, the measured V_{off} and V_{max} would change a great deal. The doping concentration can change versus position on the wafer if hot spots occur on the wafer during growth in the MBE system. As temperature increases, the sticking coefficient of the Si atoms impinging on the AlGaAs substrate is lowered and the group III to group V ratio decreases [19,47]. The result is that for a given Si flux impinging on the substrate, fewer Si atoms are incorporated as impurities. The Si atoms which do incorporate into the substrate have a greater number which go into deep levels as acceptors than at a lower temperature which tends to compensate the donors in the epitaxy [3,19,69]. Thus the amount of Si atoms incorporated decreases while compensation increases, decreasing the effective donor density of the AlGaAs from that predicted by

the flux of Si atoms impinging on the substrate.

The formation of an oxide layer under the gate could be a result of the pre-metal etch step (see appendix C) in the fabrication process or a result of the Ti layer in the gate metal reacting with the H_2O_2 in the etchant used to remove the p+ layer between the gate and the source/drain [21,74]. The oxide behaves like a dielectric, preventing gate current from leaking to the source and drain. If the oxide were of a chemically stable form, there would be no need for the Schottky barrier, but the native surface oxides on GaAs are both unstable and unreproducible. The source resistance on all of the samples in question (2373, 2376, 2377) was never greater than that found on samples 2263, 2265, or 2378, so this could be a very likely cause of the difference in barrier height. One drawback to the oxide assumption is that the gate to source resistance (R_{sg}) was often small for the values of V_{max} observed.

The voltage from source to drain on the device during the measurement of the gate I-V also has an effect on the observed V_{max}. This difference is illustrated in Fig 6-2 for sample 2265 with the left-hand I-V curve measured with V_{ds} = 0 V, and the right-hand I-V curve measured with V_{ds} = 2 V.

As can be seen the I-V curve is shifted considerably due to the addition of the voltage drop across the source resistance (R_s) For many of the later samples, the gate current measured with V_{ds} = 2 V and V_g = 2 V was less than 100μA. Thus it is important to measure the gate I-V curves with the source and drain as common, to obtain the proper results.

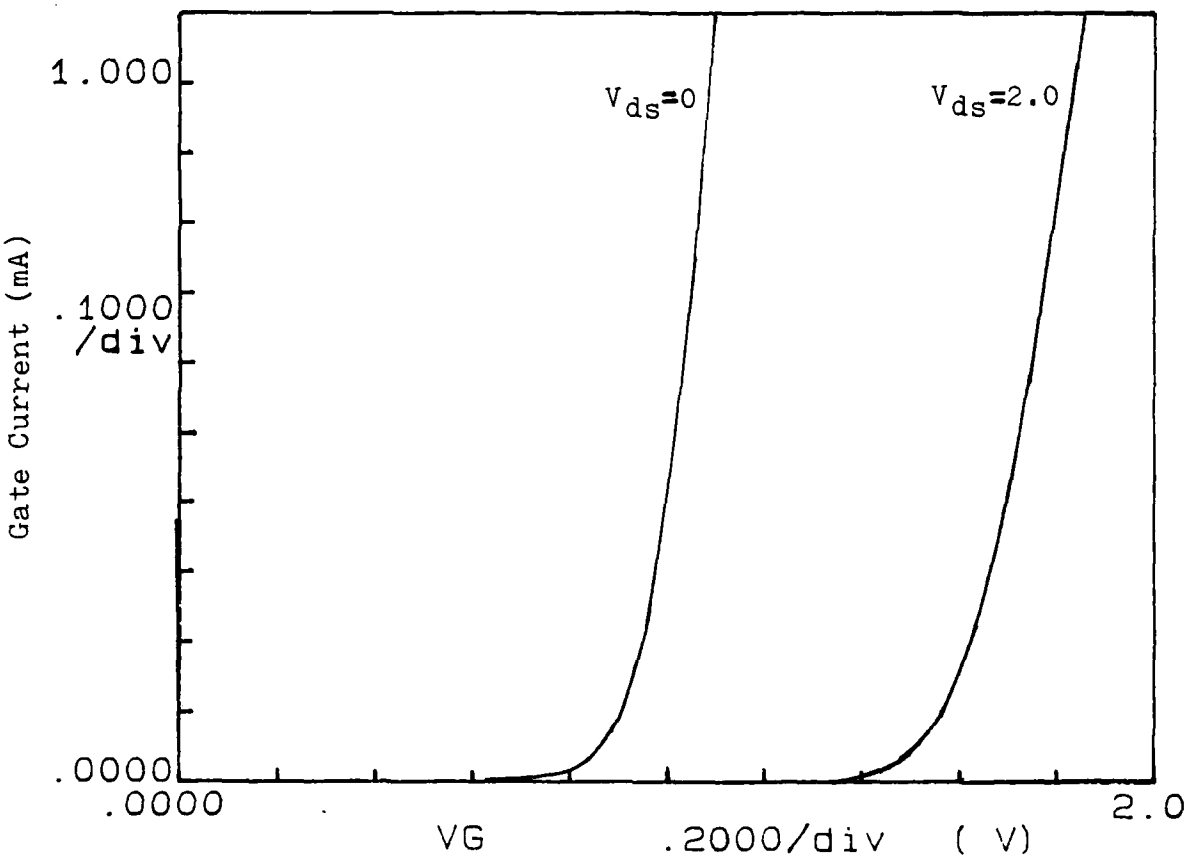
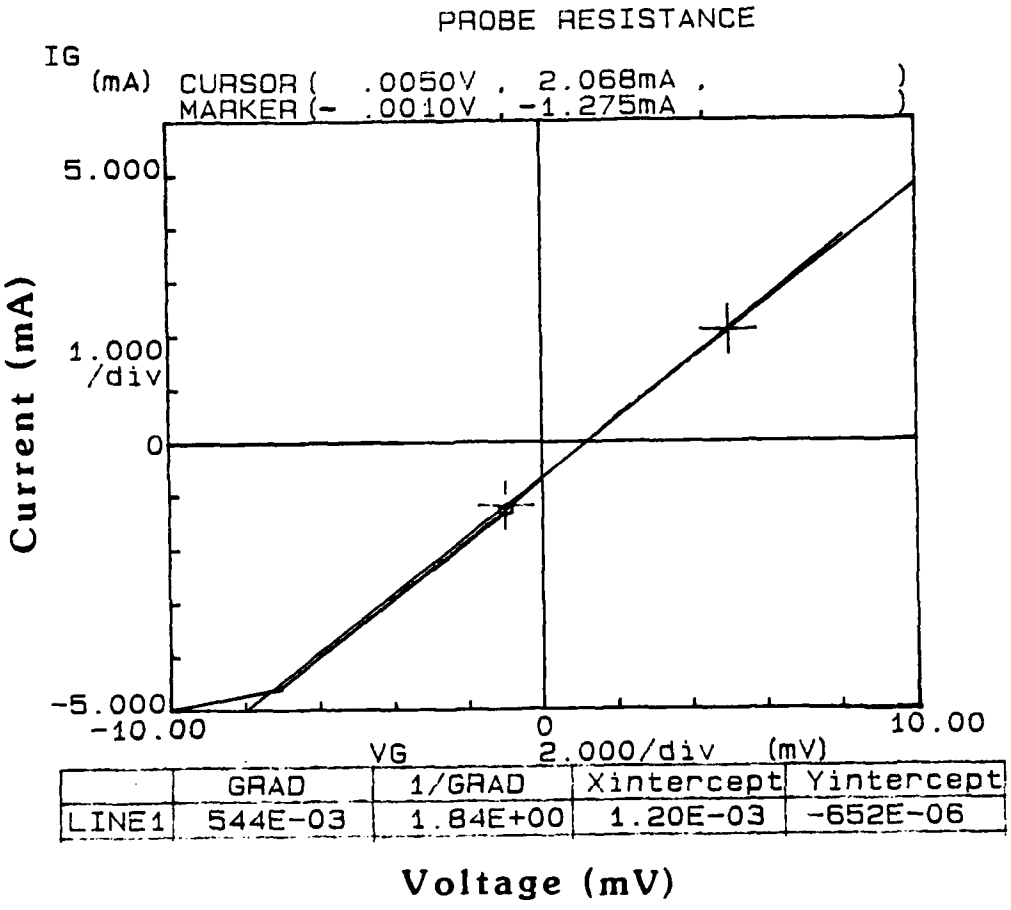


Fig 6-2 Effect of V_{ds} on Gate I-V Curves For Sample 2265.

The effect of a rectifying probe contact would be to increase the apparent barrier because the potential required to overcome the barrier is additive. This effect should be minimal as shown by the I-V curves for the probe combinations in Fig 6-3 show only a linear dependence on applied voltage.



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	544E-03	1.84E+00	1.20E-03	-652E-06

Fig 6-3 Probe I-V Curve for Two Probe and Three Probe Measurements.

The shift in V_{max} was also observed when moving from 2 m devices to 4 μm and 10 μm devices. The measured gate I-V was often lower as gate length increased, but in some cases the measured barrier increased. These differences are not readily explained, because the barrier measurement should be independent of gate length. The most likely reason is that the reaction of the H_2O_2 with the Ti is not as severe in terms of percentage of gate area damaged, for the larger gate length devices.

The barrier shift observed in Fig 6-4 for sample 2377 yielded the largest value for V_{max} (1.6 V) which is approximately the bandgap of $Al_{0.3}Ga_{0.7}As$ (1.62 V).

The enhanced Schottky barrier allows the circuit designer to place a larger gate voltage (1.6 V) on the ESMODFET than on than on the MODFET (0.8 V) before gate leakage current becomes excessive. This translates into a 3 dB increase in the signal to noise ratio for the ESMODFET before gate leakage current becomes excessive. The control sample for 2377 (no p+ layer) was used to compare the effect of the barrier shift for a device with the p+ layer from sample 2377.

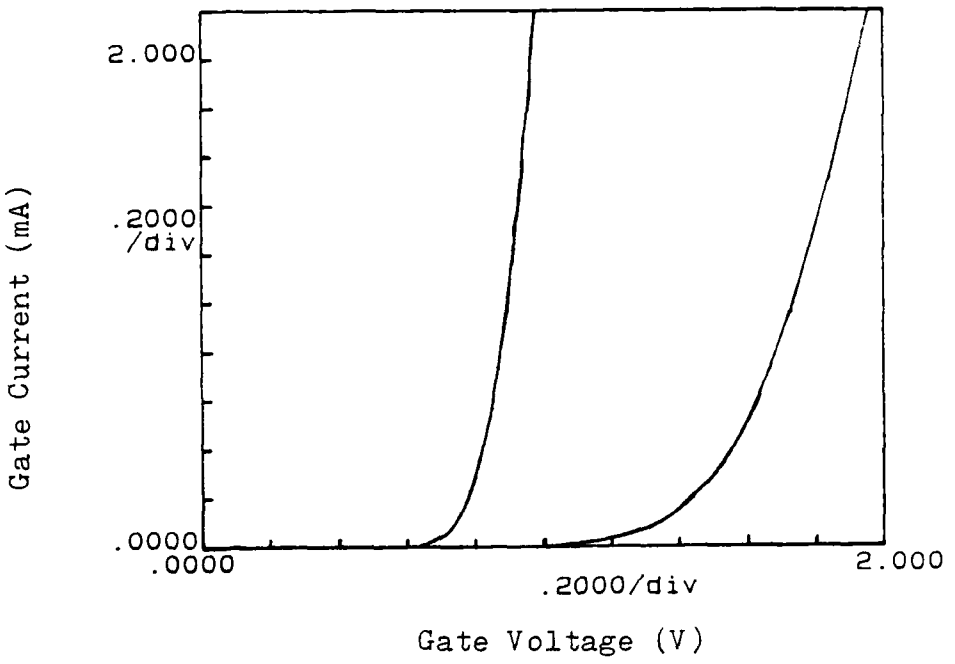


Fig 6-4 Gate I-V Curve of MODFET and ESMODFET from Sample 2377.

The effect of the gate leakage current is best illustrated in Figs 6-5 and 6-6. Figs 6-5 and 6-6 are expanded scale plots of the drain current versus drain voltage for various values of gate voltage for the MODFET and ESMODFET devices used in generating the I-V curves of Fig 6-4. The V_{max} of the MODFET is approximately 0.8 V while that of the ESMODFET is 1.6 V. This becomes apparent as Fig 6-5 is observed. As the gate voltage is shifted above 0.8 V in Fig 6-5, the drain current also shifts away from the origin. This effect is due to the Schottky barrier at the gate contact becoming forward biased and allowing current to leak past. Note in Fig 6-5 that the maximum gate voltage applied is 1.2 V. In Fig 6-6, a gate voltage of 1.2 V is applied and stepped to 1.6 V in increments of 0.2 V. The drain current curves for gate voltages of 1.2 V and 1.4 V show no shift, while the curve for a gate voltage of 1.6 V shows some shift. Thus the increased barrier due to the p+ layer is preventing the current from leaking until the ESMODFET becomes forward biased near 1.6 V. While the increased barrier available from the use of highly-doped appears promising, the large effect of doping on the actual Schottky barrier obtained must be overcome. The only way to correlate theory with experiment is to measure V_{max} and V_{off} and then calculate the effective doping. This is necessary because the doping concentrations of the GaAs and AlGaAs layers are not known precisely.

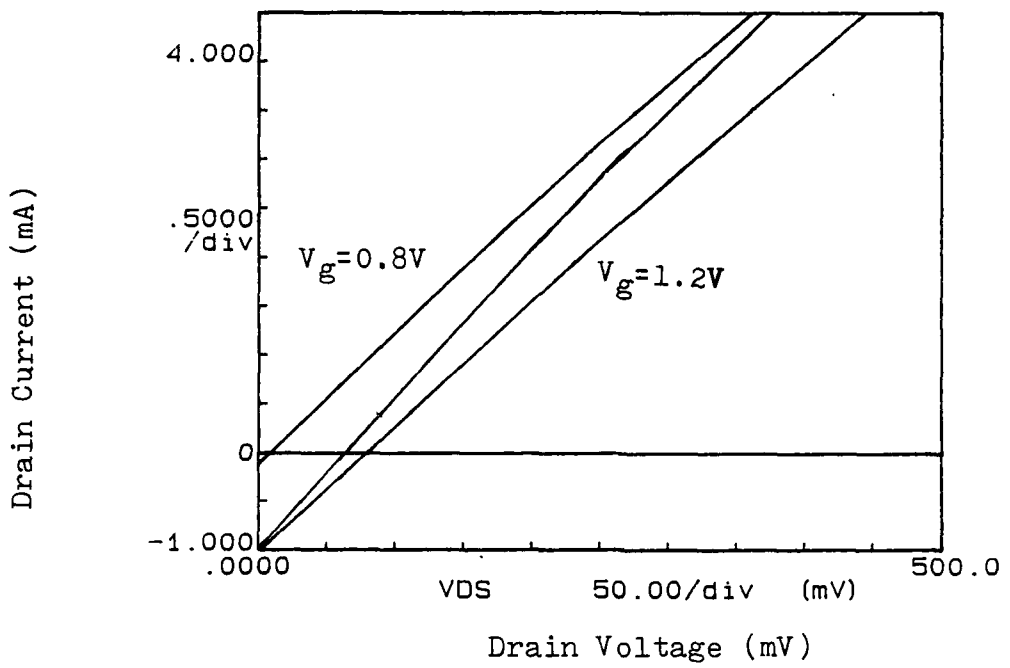


Fig 6-5 Drain Current vs Gate Voltage for MODFET from Sample 2377 Showing Shift when $V_g > V_b$.

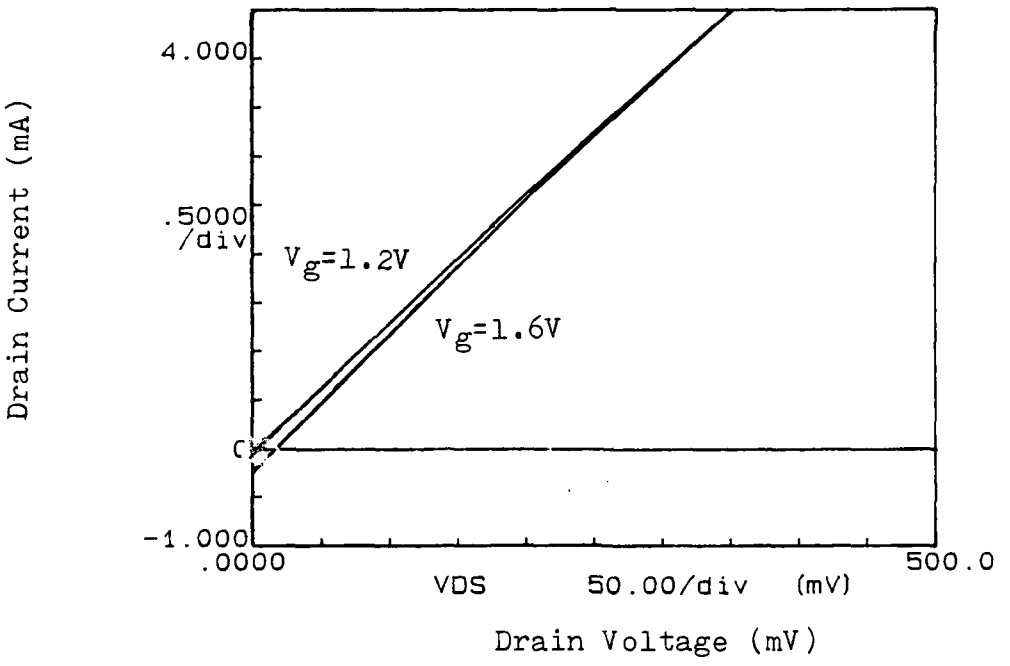


Fig 6-6 Drain Current vs Gate Voltage for ESMODFET from Sample 2377 Showing Virtually No Shift.

Effective Doping Concentration

The effective doping concentration must be determined before the comparison between theory and experiment can be made. Ideally the doping should be measured using Secondary Ion Mass Spectroscopy, Hall measurements, or C-V measurement. The technique used in this thesis was to take the results from several samples having the same doping concentrations but different layer thicknesses, and then finding the doping concentrations which matched the observed results. This involved assuming the metal barrier (V_b) was 0.8V, the thicknesses were exact, and that the mole fraction was also exact. The experimental values (See Table 6-2) for the doping concentration are also given in ranges due to the uncertainty of V_{max}.

Table 6-2 Effective Doping Concentration

Sample	Deposited		Experimental	
	N_d	N_a	N_d	N_a
2263-1A	3E18	2E19	1.1-1.3 E18	1.0-1.1 E19
2265-1A	3E18	2E19	1.0-1.3 E18	1.0-1.5 E19
2373-1A	3E18	2E19	2.3-2.4 E18	2.0-2.1 E19
2376-1A	3E18	2E19	2.0-2.1 E18	2.0-2.1 E19
2377-1A	3E18	2E19	2.2-2.3 E18	2.0-2.1 E19
2378-1A	3E18	2E19	2.4-2.5 E18	2.0-2.1 E19

E18 = 10^{18} cm^{-3}, E19 = 10^{19} cm^{-3}

As mentioned previously, temperature has a definite effect on the doping concentration [19,47]. Mole fraction also has an effect on doping concentration [3,19,69]. The typical values used for Si doping of AlGaAs are that (65-70)% of the Si atoms incorporate as donors (N_d) with approximately 30% incorporated as acceptors (N_a) for $Al_{0.3}Ga_{0.7}As$ [19,69]. The AlGaAs donor concentration (N_d) determined from experimental data for the last four samples (2373-2378) corresponds closely to that determined by the 70% rule. The first two samples (2263, 2265) show a large decrease in the doping of the GaAs (N_a) and the AlGaAs (N_d). This cannot be explained readily, but must be due to an abnormally high amount of compensation combined with the Si atoms not incorporating into the lattice.

Turn-on Voltage

The turn-on voltage (V_{off}) is also affected by the doping concentration. The measured Voff values were much more consistent across the wafer than the values found for V_{max}. The turn-on voltage was used along with the Schottky barrier to match the results with theory. The turn-on voltage is very predictable by the theory. Because the dimensions of the ESMODFET are very consistent under the gate, due to the absence of the etch required for standard MODFETs, V_{off} is consistent across the sample. Thus one advantage, in addition to an enhanced barrier, of the ESMODFET over the standard MODFET is that V_{off} is very consistent across the wafer increasing the yield for a given V_{off} over the standard process used to fabricate MODFETs.

Fabrication

The fabrication process is a major factor in the final analysis due to the etch step required to remove the GaAs layer in the regions between the gate and source/drain. If the etchant is not prepared properly, too much material can be etched away making the AlGaAs layer too thin allowing the surface states to deplete the 2DEG or else removing the dopant available to the 2DEG in regions between the gate and the source and drain. The effective doping also enters into the picture, because if the doping is less than the value used to predict the required thickness of the AlGaAs, depletion could still occur even if the etch is correctly applied. One complete series of devices was found to be defective due to overetching. The bad devices showed an extremely high contact resistance (>10K) which can only be explained by the lack of the 2DEG between the source/drain and gate. The etchant also reacts with Ti as is demonstrated in Fig 6-7. The H_2O_2 in the etchant (see Appendix C) reacts with Ti either dissolving the Ti or causes large sections of the Au to lift-off.

The etch used to remove the GaAs layer for samples 2263 and 2265 (NH_4OH:H_2O_2:DI Water) is extremely fast, removing GaAs at 17Å per second. The etch is also pH dependent, etching faster if the pH is low and slightly slower if the pH is higher while lessening the ability of AlGaAs to stop the etch when the pH is low. The problem with the series of samples which were overetched was traced to a bad pH meter. The pH was undoubtably too low thus the

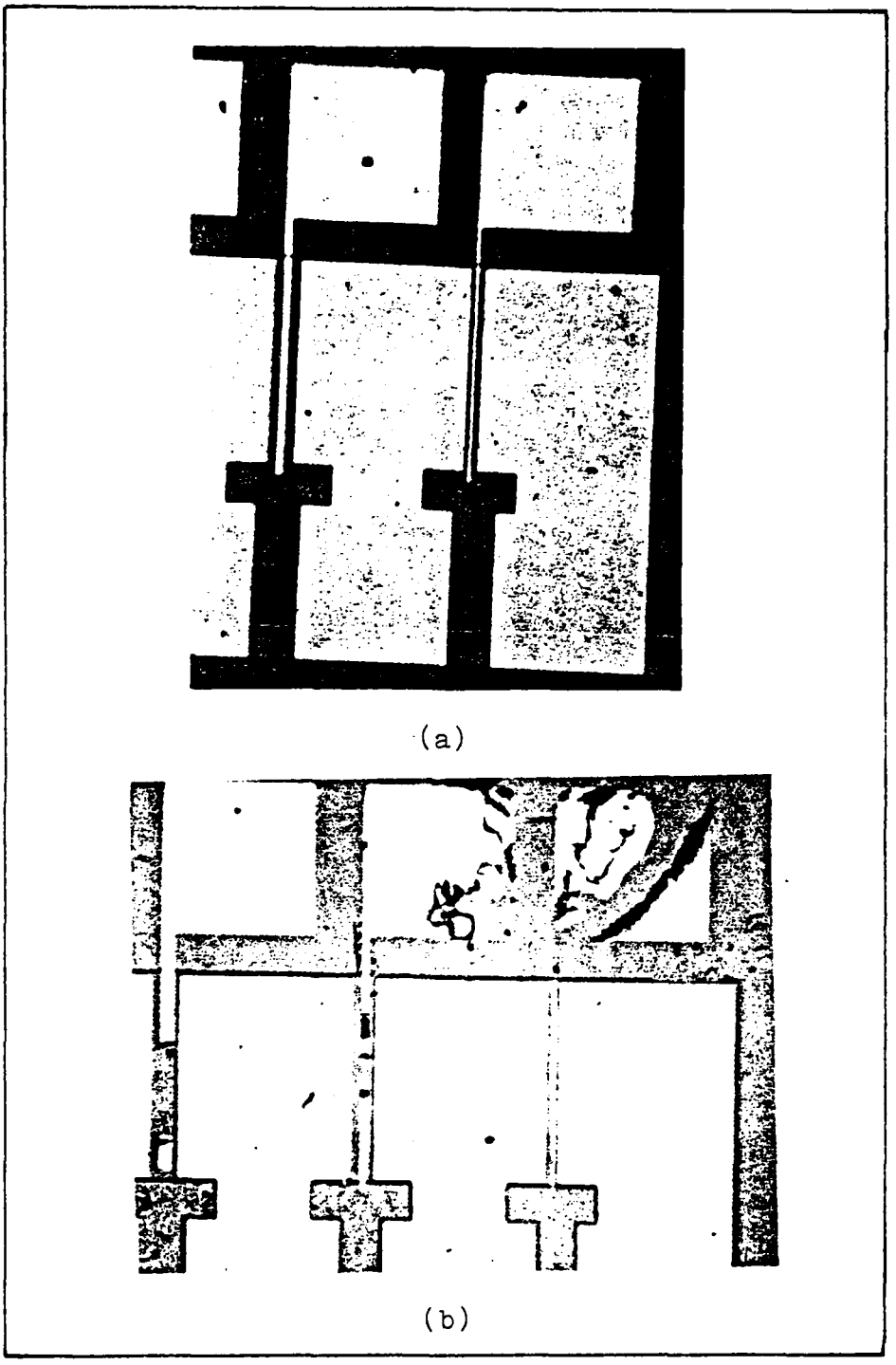


Fig 6-7 Effect of Slow Etchant on Ti Gate of ESMODFET
a) Before Etching
b) After 15 Seconds in Slow Etch

overetch occured. Another factor is that the etch may not etch at a constant rate, etching AlGaAs much faster initially, while slowing down after a period of time. The etch rates were determined for thick samples and then averaged, possibly hiding the effect. The etchant can also be made with higher pH values. A pH of 7.2 for the etch will result in a 16Å per second etch of GaAs and a 0.3Å per second etch of AlGaAs [21]. Thus it is much better to have a pH which is higher than 7.05 rather than a pH which is less than 7.05.

A slower etch (Bell Labs proprietary) with a 3Å per second etch rate was also prepared. This etchant was used on several samples in an attempt to gain better control for the etch step. The slow etch also brought out the problems with the Ti gate metal. The sample shown in Fig 6-7 was etched for 15 seconds in the slower etch versus 7 seconds in the pH 7.05 etch. After close examination of the other samples, the effect of the H_2O_2 was also noticeable on the samples etched with the pH 7.05 etch. The etch could be changed to one which does not react with Ti, but the better solution may be to find a suitable gate metal which does not react with the etchant. Another alternative would be to add a photoresist step to protect the gate metal during the etch step.

VII Conclusions and Recommendations

Conclusions

Based on the results of this thesis the following conclusions can be made:

1. The Schottky barrier of the MODFET can be altered in a predictable manner through the use of highly doped surface layers. A barrier shift from 0.8V to 1.6V was obtained using a p+ surface layer.
2. The contact resistance of the ESMODFET is comparable to that of the MODFET.
3. The fabrication process is still experimental and extremely critical to the operation of the ESMODFET.
4. The precise control required for doping concentration can be a disadvantage due to the wide variation in Schottky barrier height for different doping concentrations.
5. The effective doping of the p+ and AlGaAs layer must be known to accurately compare results with theory.
6. The slow etch reacted with the Ti gate metal causing damage to the metal and deleterious effects to the Schottky barrier.
7. The transconductance of the ESMODFET and MODFET are similar. No major reduction was measured.

Recommendations

The following recommendations are suggested for future study of the ESMODFET:

1. Measuring the Schottky barrier height using an optical technique. This data can be compared to the Schottky barrier found in this thesis using I-V measurements.
2. Testing the microwave performance of the ESMODFET and comparing it to a MODFET with a similar turn-on voltage. Perform such tests not only for the 2 μm gate length devices used in this thesis but also for 1 μm and submicron devices.
3. Measure the temperature sensitivity of the ESMODFET. The Schottky barrier is temperature dependent. The effect of temperature on the overall performance of the ESMODFET should be characterized.
4. Use an ion-implantation technique to deposit the p+ layer under the gate contact. This would eliminate the etch step which is extremely critical. Transient annealing would prevent the Si in the AlGaAs from diffusing into the 2DEG.
5. Make several samples with the thickness of the p+ GaAs layer as the only variable for a given AlGaAs layer thickness and doping concentration. Then plot the family of curves and compare with theory.
6. Find the maximum barrier height available for typical MODFET layer thicknesses.

7. Measure the mobility and 2DEG concentration of the ESMODFET using Hall and C-V measurements.
8. Explore the use of different gate metals to reduce the etchant reaction observed with Ti.
9. Explore the use of alternative selective etchants which are more controllable without the deleterious effects on the deposited gate metal.
10. Due to the added p+ layer, the gate capacitance should be lower for the ESMODFET. The gate capacitance should be measured and then compared to a MODFET with a similar turn-on voltage. The effect of the gate capacitance on microwave performance should also be considered.

Appendix A

Derivation of Barrier Height for Metal-p+(GaAs)-n(AlGaAs) System From Poisson's Equation

The method commonly used to describe metal-semiconductor and semiconductor-semiconductor junctions is based on the depletion approximation, which assumes that Poisson's equation is valid for tne system involved. The system to be solved using the depletion approximation is given below in Fig A-1.

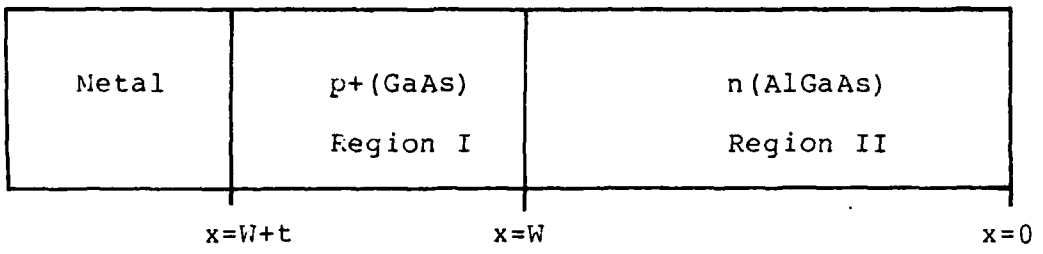


Fig A-1 Metal-Semiconductor System of p+ MODFET

Poisson's equation in region II is given by:

$$\frac{\partial^2 \psi}{\partial x^2} = \frac{-\rho}{\epsilon_2} \qquad \text{(A-1)}$$

where ρ = charge density

ϵ_2 = permittivity of AlGaAs

for n-type semiconductor material

$$\rho = q N_d \qquad \text{(A-2)}$$

where q = electronic charge

N_d = doping of AlGaAs layer

which leads to

$$\frac{\partial^2 \psi}{\partial x^2} = \frac{-q N_d}{\epsilon_2} \qquad \text{(A-3)}$$

Integrating Poisson's equation to obtain the electric field in Region II yields

$$E_2 = \frac{-qN_d x}{\epsilon_2} + C_1 \qquad \text{(A-4)}$$

But at some distance W into the AlGaAs the electric field and the electrsotatic potential must equal zero. This is depicted in Fig A-2. Defining the point $x = 0$ at the depletion depth W into the AlGaAs and the point $x = W+t$ for the metal-p+ junction simplifies the solution to all boundary conditions. Thus at $x = 0$ C_1 must equal zero providing the solution for the electric field in Region II.

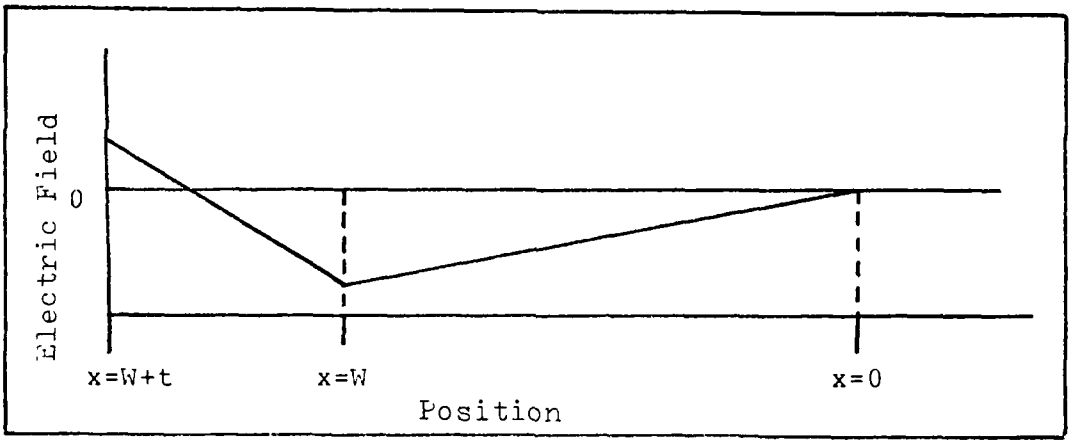


Fig A-2 Electric Field vs Position

Thus the electric field in Region II is given by

$$E_2 = \frac{-qN_d x}{\epsilon_2} \quad (0 \le x \le W) \qquad \text{(A-5)}$$

But Gauss' Law forces the electric field to be continuous at $x = W$ with the relationship

$$\epsilon_1 E_1 = \epsilon_2 E_2 \qquad \text{(A-6)}$$

For Region I Poisson's equation is given by

$$\frac{\partial^2 \psi}{\partial x^2} = \frac{q N_a}{\epsilon_1} \qquad \text{(A-7)}$$

where $-qN_a$ = charge density p+ GaAs

ϵ_1 = permittivity of GaAs

Integrating Eq A-7 leads to

$$E_1 = \frac{q N_a x}{\epsilon_1} + C_2 \quad (W \le x \le W+t) \qquad \text{(A-8)}$$

Using Eq A-6 the solution for C_2 can be found

$$C_2 = \frac{-qW}{\epsilon_1}(N_a + N_d) \qquad \text{(A-9)}$$

Substituting for C_2 yields

$$E_1 = \frac{qN_a}{\epsilon_1}(x-W) - \frac{qN_dW}{\epsilon_1} \quad (W \le x \le W+t) \qquad \text{(A-10)}$$

Solving for the electrostatic potential using the relation

$$\psi(x) = -\int E(x)\,dx \qquad \text{(A-11)}$$

Integrating Eq A-5 for Region II yields

$$\psi_2 = \frac{qN_d x^2}{2\epsilon_2} + C_3 \qquad \text{(A-12)}$$

But at x=0 the electrostatic potential is zero. Thus

$$C_3 = 0 \tag{A-13}$$

Thus the electrostatic potential for Region II is given by

$$\psi_2(x) = \frac{q N_d x^2}{2\epsilon_2} \quad (0 \le x \le W) \tag{A-14}$$

In a p-n semiconductor junction with both semiconductors having equal bandgaps $\psi_1(W)=\psi_2(W)$. But, because of the conduction band discontinuity (ΔE_c) between AlGaAs and GaAs

$$\psi_1(W) = \psi_2(W) - \Delta E_c \tag{A-15}$$

Integrating Eq A-10 to obtain the electrostatic potential yields

$$\psi_1(x) = -\left[\frac{q N_a}{\epsilon_1}\left(\frac{x^2}{2} - Wx\right) - \frac{q N_d W x}{\epsilon_1}\right] + C_4 \tag{A-16}$$

which when x = W yields

$$\frac{q N_d W^2}{2\epsilon_2} - \Delta E_c = \frac{-q N_a}{\epsilon_1}\left(\frac{W^2}{2} - W\right) + \frac{q N_d W^2}{\epsilon_1} + C_4 \tag{A-17}$$

Rearranging terms to solve for C_4

(A-18)

Substituting for C in Eq A-16 and rearranging terms

$$\psi_1(x) = \frac{-q N_a}{2\epsilon_1}\left(x^2 - 2Wx + W^2\right) - \Delta E_c + \frac{q N_d W(x-W)}{\epsilon_1} + \frac{q N_d W^2}{2\epsilon_2} \tag{A-19}$$

Which finally reduces to

$$\psi_1(x) = -\frac{q N_a}{2\epsilon_1}(x-W)^2 + \frac{q N_d W}{\epsilon_1}(x-W) + \frac{q N_d W^2}{2\epsilon_2} - \Delta E_c \quad (W \le x \le W+t) \tag{A-20}$$

AD-A164 103 STUDY AND ANALYSIS OF ALGAAS/GAAS MODULATION DOPED FIELD-EFFECT TRANSISTO..(U) AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH SCHOOL OF ENGI.. K L PRIDDY 2/2

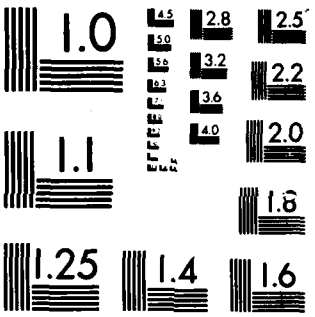
UNCLASSIFIED DEC 85 AFIT/GEO/ENG/85D-1 F/G 9/5 NL

END

FILMED

4-86

DTIC



MICROCOPY RESOLUTION TEST CHART

NATIONAL BUREAU OF STANDARDS-1963-A

Which must equal the Schottky barrier at x = W+t. Thus

$$V_b - V_g = \frac{-qN_a t^2}{2\epsilon_1} + \frac{qN_d W t}{\epsilon_1} + \frac{qN_d W^2}{2\epsilon_2} - \Delta E_c \qquad \text{(A-21)}$$

Which is the same expression as Eq 2-3.

APPENDIX B

Derivation of Schottky Barrier Height for the ESMODFET From Poisson's Equation

The derivation used in this appendix assumes that all of the available donors and acceptors in the semiconductor layers are ionized. The other assumptions are that the electric field in the quantum well is quasi-constant and equal to qN_s/ϵ_1 [13,15], and that the potential at the undoped AlGaAs-GaAs heterojunction is given by E_c-E_{fi} [13,15].

The stucture of the ESMODFET under the gate is given by Fig B-1 below.

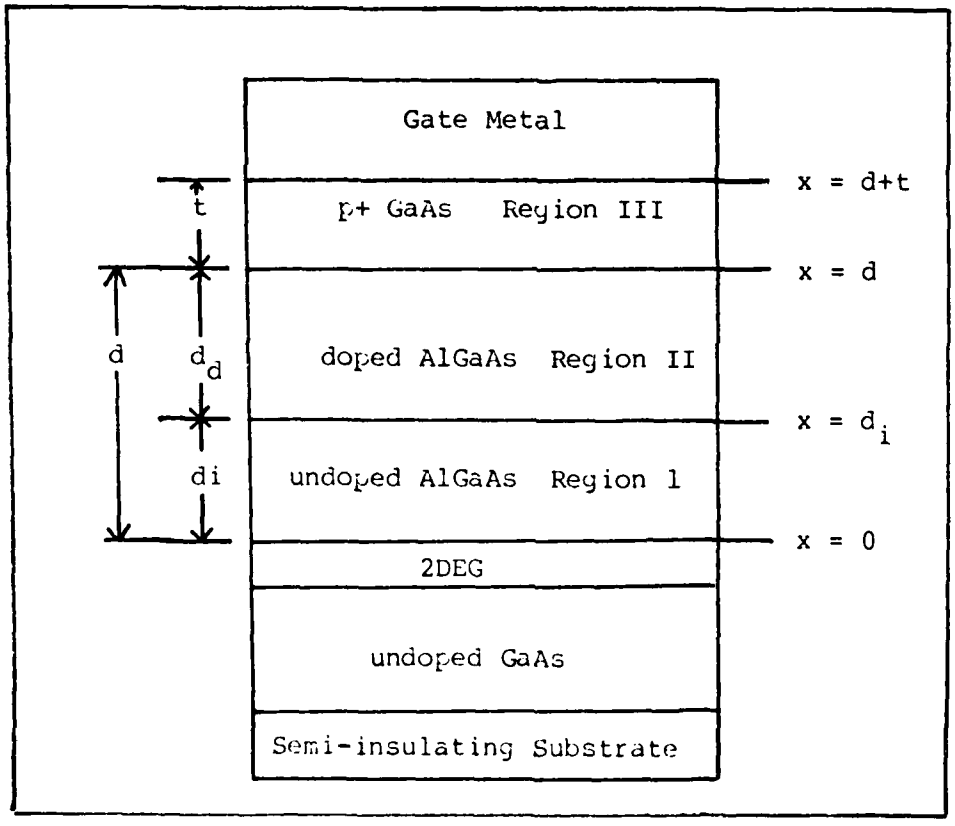


Fig B-1. ESMODFET Structure Under the Gate Contact.

The solution of Poisson's equation in each region, combined with appropriate boundary conditions will yield the electric field and electrostatic potential for each region of the ESMODFET. Starting at the $x = 0$ point and moving toward the $x = d+t$ point to solve for the electric field and electrostatic potential.

Region I $(0 < x < d_i)$

Boundary Condition

$$\epsilon_2 E_1 = \epsilon_1 E_o \tag{B-1}$$

where ϵ_1 = permittivity of GaAs

ϵ_2 = permittivity of AlGaAs

E_o = Electric field in 2DEG

E_1 = Electric field in Region I

Using the assumption that the electric field is quasi-constant in the 2DEG

$$E_o = \frac{q n_s}{\epsilon_1} \tag{B-2}$$

and substituting for E_0 in Eq B-1 yields

$$\epsilon_2 E_1 = q n_s \tag{B-3}$$

By integrating Poisson's equation the electric field in Region I can be found

$$\int \frac{\partial^2 \psi}{\partial x^2} = \int \frac{-\rho}{\epsilon_2} \tag{B-4}$$

which leads to

$$E_1 = \frac{-\rho x}{\epsilon_2} + C_1 \tag{B-5}$$

But because the AlGaAs is undoped in Region I $(\rho \approx 0)$

$$E_1 = C_1 \tag{B-6}$$

Matching boundary conditions at x = 0, we find

$$E_1 = \frac{q n_s}{\epsilon_2} \tag{B-7}$$

which yields

$$E_1(x) = \frac{q n_s}{\epsilon_2} \quad (0 \leq x \leq d_i) \tag{B-8}$$

Region II $(d_i < x < d)$

Boundary Condition:

$$E_1(d_i) = E_2(d_i) \tag{B-9}$$

where E_1 = Electric field in Region I.

E_2 = Electric field in Region II.

From Poisson's Equation, we obtain the following

$$\frac{\partial^2 \psi}{\partial x^2} = \frac{-q N_d}{\epsilon_2} \tag{B-10}$$

integrating Eq B-10

$$E_2 = \int \frac{-q N_d}{\epsilon_2} \, dx \tag{B-11}$$

which leads to

$$E_2 = \frac{-q N_d x}{\epsilon_2} + C_2 \tag{B-12}$$

Applying the boundary condition at x = d_i

$$C_2 - \frac{qN_d d_i^o}{\epsilon_2} = \frac{q n_s}{\epsilon_2} \qquad \text{(B-13)}$$

therefore

$$C_2 = \frac{q n_s}{\epsilon_2} + \frac{qN_d d_i^o}{\epsilon_2} \qquad \text{(B-14)}$$

which yields

$$E_2 = -\frac{qN_d}{\epsilon_2}(x - d_i^o) + \frac{q n_s}{\epsilon_2} \quad (d_i^o \le x \le d) \qquad \text{(B-15)}$$

Region III (d < x < d + t)

Boundary Condition

$$\epsilon_2 E_2(d) = \epsilon_1 E_3(d) \qquad \text{(B-16)}$$

where E_3 = Electric field in Region III

From Poisson's equation, we obtain

$$\frac{\partial^2 \psi}{\partial x^2} = \frac{qN_a}{\epsilon_1} \qquad \text{(B-17)}$$

$$E_3 = \frac{qN_a x}{\epsilon_1} + C_3 \qquad \text{(B-18)}$$

but at x = d

$$\epsilon_1 \left[\frac{qN_a d}{\epsilon_1} + C_3\right] = \epsilon_2 \left[\frac{q n_s}{\epsilon_2} - \frac{qN_d d_d}{\epsilon_2}\right] \qquad \text{(B-19)}$$

which yields

$$C_3 = \frac{q n_s}{\epsilon_1} - \frac{qN_d d_d}{\epsilon_1} - \frac{qN_a d}{\epsilon_1} \qquad \text{(B-20)}$$

which leads to the final result

$$E_3(x) = \frac{qN_a(x-d)}{\epsilon_1} - \frac{qN_d d_d}{\epsilon_1} + \frac{q n_s}{\epsilon_1} \quad (d \le x \le d+t) \qquad \text{(B-21)}$$

The electric field within the ESMODFET is shown in Fig B-2.

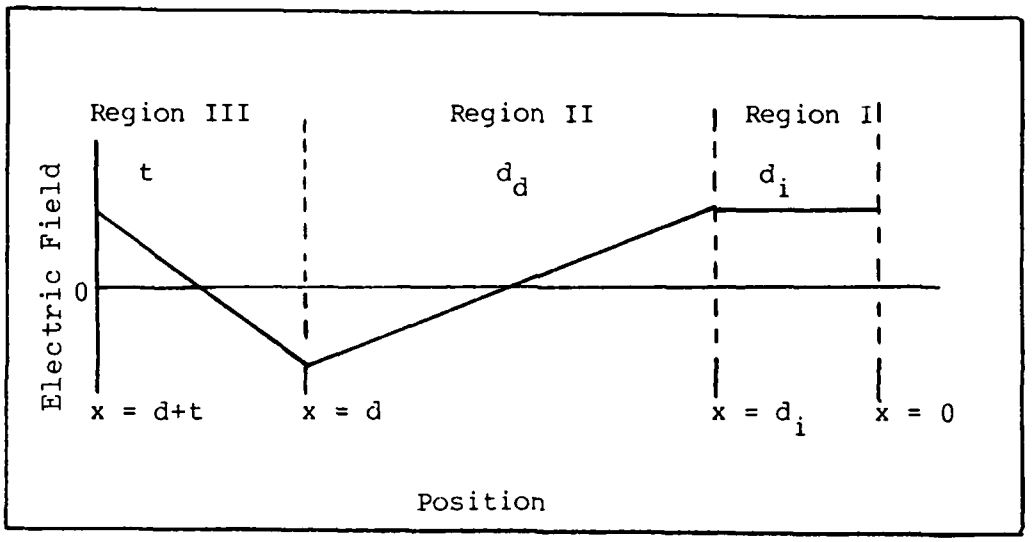


Fig B-2 Electric Field vs Position in ESMODFET

The electrostatic potetial for each region of the ESMODFET is found by integrating the electric field using the relation

$$\Psi(x) = -\int E(x)\,dx \tag{B-22}$$

Region I $(0 < x < d_i)$

Boundary Condition

$$\Psi_1(0) = \Delta E_c - E_{Fi} \tag{B-23}$$

Integrating the electric field

$$\Psi_1(x) = -\int \frac{q n_s}{\epsilon_2}\,dx \tag{B-24}$$

which yields

$$\Psi_1(x) = -\frac{q n_s x}{\epsilon_2} + C_4 \tag{B-25}$$

but at x = 0

$$\Psi_1(0) = \Delta E_c - E_{Fi} = C_4 \tag{B-26}$$

which yields

$$\Psi_1(x) = -\frac{q n_s x}{\epsilon_2} + \Delta E_c - E_{Fi} \quad (0 \le x \le d_i) \tag{B-27}$$

Region II ($d_i < x < d$)

Boundary condition

$$\Psi_1(d_i) = \Psi_2(d_i) \tag{B-28}$$

integrating the electric field

$$\Psi_2 = -\int \left(\frac{q n_s}{\epsilon_2} - \frac{q N_d (x - d_i)}{\epsilon_2} \right) dx \tag{B-29}$$

which yields

$$\Psi_2(x) = -\frac{q n_s x}{\epsilon_2} + \frac{q N_d}{2\epsilon_2} (x - 2d_i) x + C_5 \tag{B-30}$$

but

$$\Psi_1(d_i) = \Psi_2(d_i) \tag{B-31}$$

matching the electrostatic potential at $x = d_i$

$$-\frac{q n_s d_i}{\epsilon_2} + \Delta E_c - E_{Fi} = -\frac{q n_s d_i}{\epsilon_2} + \frac{q N_d}{2\epsilon_2} (d_i - 2d_i) d_i + C_5 \tag{B-32}$$

which yields the constant of integration

$$C_5 = \frac{q N_d d_i^2}{2\epsilon_2} + \Delta E_c - E_{Fi} \tag{B-33}$$

substituting for C_5

$$\Psi_2(x) = \frac{qN_d(x-2d_i)x}{2\epsilon_2} + \frac{qN_d d_i^2}{2\epsilon_2} + \Delta E_c - E_{Fi} - \frac{qn_s x}{\epsilon_2} \qquad \text{(B-34)}$$

Rearranging terms yields

$$\Psi_2(x) = \frac{qN_d}{2\epsilon_2}(x-d_i)^2 - \frac{qn_s x}{\epsilon_2} + \Delta E_c - E_{Fi} \quad (d_i \leq x < d) \qquad \text{(B-35)}$$

Region III (d < x < d+t)

Boundary condition

$$\Psi_3(d) = \Psi_2(d) - \Delta E_c \qquad \text{(B-36)}$$

Integrating the electric field

$$\Psi_3(x) = -\int\left(\frac{qN_a(x-d)}{\epsilon_1} + \frac{qn_s}{\epsilon_1} - \frac{qN_d d_d}{\epsilon_1}\right)dx \qquad \text{(B-37)}$$

$$\Psi_3(x) = \frac{-qN_a}{2\epsilon_1}(x-2d)x - \frac{qn_s x}{\epsilon_1} + \frac{qN_d d_d x}{\epsilon_1} + C_6 \qquad \text{(B-38)}$$

the electrostatic potential at x = d is given by

$$\Psi_2(d) = \frac{qN_d d_d^2}{2\epsilon_2} + \Delta E_c - E_{Fi} - \frac{qn_s d}{\epsilon_2} \qquad \text{(B-39)}$$

$$\Psi_3(d) = \frac{qN_a d^2}{2\epsilon_1} - \frac{qn_s d}{\epsilon_1} + \frac{qN_d d_d d}{\epsilon_1} + C_6 \qquad \text{(B-40)}$$

Applying the boundary condition at x = d and solving for C_6

$$C_6 = \frac{qN_d d_d^2}{2\epsilon_2} - \frac{qn_s d}{\epsilon_2} + \frac{qn_s d}{\epsilon_1} - E_{Fi} - \frac{qN_a d^2}{2\epsilon_1} - \frac{qN_d d_d d}{\epsilon_1} \qquad \text{(B-41)}$$

Substituting for C_6 yields

$$\psi_3(x) = \frac{-q N_a (x-d)^2}{2\epsilon_1} - \frac{q n_s (x-d)}{\epsilon_1} + \frac{q N_d d_d (x-d)}{\epsilon_1} + V_{max} - \Delta E_c \quad \text{(B-42)}$$

where

$$V_{max} \equiv \Delta E_c - E_{fi} - \frac{q n_s d}{\epsilon_2} + \frac{q N_d d_d^2}{2\epsilon_2} \quad \text{(B-43)}$$

Plotting the electrostatic potential versus position yields the conduction band diagram of the ESMODFET as shown in Fig B-3.

Solving the electrostatic potential at the metal interface (x = d+t) yields

$$V_b - V_g = \frac{-q N_a t^2}{2\epsilon_1} + \frac{q N_d d_d t}{\epsilon_1} + \frac{q N_d d_d^2}{2\epsilon_2} - \frac{q n_s}{\epsilon_2}\left(d + \frac{\epsilon_2 t}{\epsilon_1}\right) - E_{fi} \quad \text{(B-44)}$$

substituting for E_{fi} [49]

$$E_{fi} = a n_s + E_{fo} \quad \text{(B-45)}$$

where $a = 1.25 \times 10^{-13}$ Vcm^{-2}

$E_{fo} = 0$ @ 300 K, 25 mV @ 77 K

$$V_b - V_g = \frac{-q N_a t^2}{2\epsilon_1} + \frac{q N_d d_d t}{\epsilon_1} + \frac{q N_d d_d^2}{2\epsilon_2} - \frac{q n_s}{\epsilon_2}\left[d + \frac{\epsilon_2 t}{\epsilon_1} + \frac{\epsilon_2 a}{q}\right] - E_{fo} \quad \text{(B-46)}$$

Rearranging in terms of n_s

$$n_s = \frac{\epsilon_2}{q\left(d_i + d_d + \frac{\epsilon_2 a}{q}\right)}\left[V_g - V_b - \frac{q N_a t^2}{2\epsilon_1} + \frac{q N_d d_d t}{\epsilon_1} + \frac{q N_d d_d^2}{2\epsilon_2} - E_{fo}\right] \quad \text{(B-47)}$$

which can be rewritten as

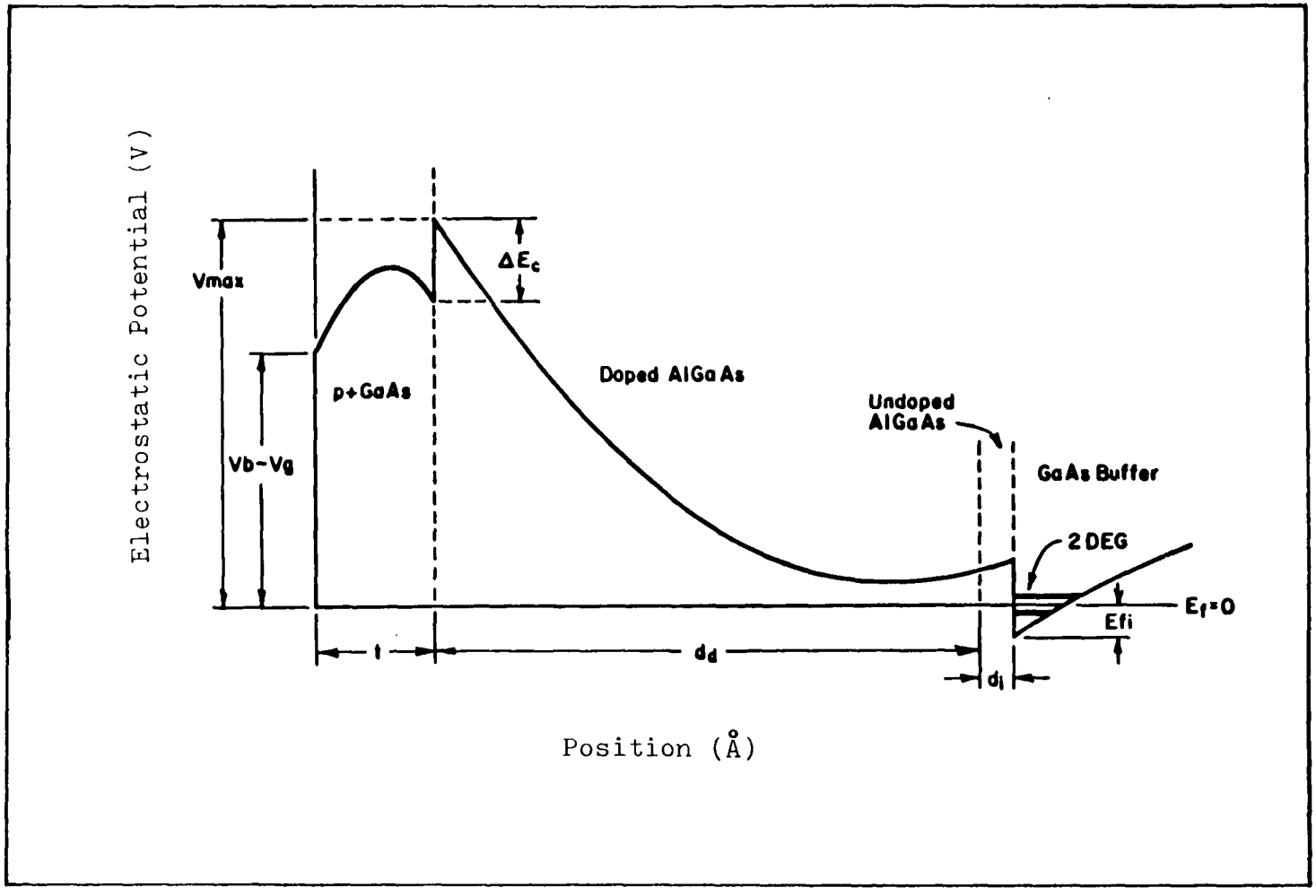


Fig B-3. Electrostatic Potential vs Position for ESMODFET

$$n_s = \frac{\epsilon_2}{q(d'+\Delta d)}\left[V_g - V_{OFF}'\right] \tag{B-48}$$

where

$$V_{OFF}' \equiv V_b + \frac{qN_a t^2}{2\epsilon_1} - \frac{qN_d d_d^2}{2\epsilon_2} - \frac{qN_d d_d t}{\epsilon_1} + E_{F_0} \tag{B-49}$$

$$\Delta d \equiv \frac{\epsilon_2 a}{q} \approx 80\,\text{Å} \tag{B-50}$$

$$d' \equiv d_d + d_i + \frac{\epsilon_2}{\epsilon_1} t \tag{B-51}$$

The final form for n_s as found in Eq B-48 is similar to that of Morkoc [49] and others [35] for the standard MODFET.

The normal MODFET 2DEG concentration (n_s) is given by

$$n_s = \frac{\epsilon_2}{q(d+\Delta d)}\left[V_g - V_{OFF}\right] \tag{B-52}$$

where

$$d \equiv d_d + d_i \tag{B-53}$$

$$V_{OFF} \equiv V_b - \Delta E_c - \frac{qN_d d_d^2}{2\epsilon_2} + E_{F_0} \tag{B-54}$$

Thus the standard charge control model can be used for ESMODFETs by simply replacing V_{off} with V_{off}' and d with d'.

APPENDIX C

Fabrication Procedure for the ESMODFET

Fabrication Procedure for Samples

Initial Inspection

Inspect wafer under microscope. Comment on surface of wafer (scratches, marks, rings, granularity, etc.).

Indium Removal

1. Prepare a solution of 1 gm $HgCl_2$ in 10 ml Dimethyl Forma mide. Gloves should be worn. Bulk quantities are usually made before processing wafers.
2. Place wafer sample in the solution and allow to soak. Occasionally place beaker with samples in ultrasonic tank and allow to vibrate for 20 seconds.
3. Occasionally remove sample from beaker and rinse with methanol. Return sample to beaker.
4. Repeat steps 2 and 3 until indium is removed. Process normally takes three to five minutes.
5. When indium is removed, remove wafer and rinse with methanol.
6. Dip a Q-tip in Alconox cleanser and lightly scrub the wafer to remove any mercury residue. Do not press when scrubbing the wafer.
7. Rinse wafer thoroughly in deionized (DI) water.
8. Blow wafer dry with filtered dry nitogen.
9. Place wafer on spinner. Turn on vacuum to hold wafer in place.
10. Apply several drops of AZ-1350J-SF photoresist to wafer and spin at 5000 rpm for 30 sec.

11. Bake in 110°C oven for 30 min.

12. Mount wafer to lapping block with paraffin, insuring that the back surface of the wafer (dull side) is facing outward.

13. Place 5 μm grit on lapping surface. Sprinkle DI water on grit to form a thick solution.

14. Place sample on lapping block down on lapping surface. Using a figure-eight motion grind the surface of the wafer until a thickness of 350 μm is obtained. The surface of the wafer should now be smooth.

15. Melt paraffin by heating with a 500W infra-red lightbulb. Remove paraffin with tweezers.

16. Remove any remaining paraffin from wafer by rinsing with trichloroethane.

17. Strip photoresist (PR) using Acetone, Methanol, and DI water.

18. Blow dry with filtered, high purity dry nitrogen or preferably with boil-off N_2 from liquid N_2 tank.

Mesa Etch

1. Prebake in 110°C oven for 5 minutes.
2. Apply AZ-1350 photoresist.
3. Spin for 30 seconds at 5000 rpm.
4. Softbake in 90°C oven for 20 minutes.
5. Expose PR for 6 sec with intensity of 8.7 mW/cm^2 .
6. Develop for 60 seconds (1:5;AZ 351 Developer:DI water).
7. Etch for 5 sec (3:1:1;DI water:H_2O_2:HF). Be sure to use gloves.

8. Rinse wafer in DI water.

9. Strip photoresist (Acetone,Methanol,DI water).

10. Blow dry with filtered dry nitrogen.

Applying Source and Drain Contacts

1. Prebake 110° C for 5 minutes.

2. Apply AZ 1350 photoresist. Spin 30 seconds at 5000 rpm.

3. Softbake 90° C for 20 minutes.

4. Expose 6 seconds at intensity of 8.7 mW/cm^2 .

5. Develop photoresist for 60 seconds (1:5;AZ 351:DI water).

6. Pre-metal clean. Dip wafer in (1:20;NH_4OH:DI water) for 20 seconds. Removes photoresist from source and drain regions.

7. Rinse in DI water and blow dry with filtered dry nitrogen.

8. Mount wafer in evaporation chamber.

9. Place Au,AuGe, and Ni pellets in crucibles.

10. Lower bell jar and insure the seal is good.

11. Lower pressure to 10^{-6} torr.

12. Deposits layers sequentially. First 600Å AuGe, then 100Å Ni, then 100Å Au. Total thickness of 1100Å.

13. Remove wafers from chamber.

14. Lift-off metal with acetone soak while occasionally dipping beaker with wafer in ultrasonic tank. Process takes 5-10 minutes.

15. Strip photoresist and blow dry with dry nitrogen.

Alloying Source and Drain Contacts

1. Insure alloying oven is profiled and heated to 500° C.

2. Purge alloying oven with nitrogen.

3. Caution must be used to insure you do not contaminate the oven. Gloves should be used. Never touch the quartz boat or the tube which pushes it into the oven without gloves. Place wafer on quartz boat and place in tube but not into oven.

4. Purge oven with nitrogen for 3 minutes.

5. Push boat into oven and heat for 50 seconds.

6. Pull boat back into tube.

7. Purge oven for 3 minutes.

8. Remove wafer from oven and then from boat.

Applying Gate Contact

1. Rinse wafer in DI water.

2. Prebake at 110° C 5 minutes.

3. Apply AZ 4110 photoresist.

4. Spin 30 seconds at 5000 rpm.

5. Softbake 90° C for 20 minutes.

6. Expose 7.5 seconds at 8.7 mW/cm^2 .

7. Soak in chlorobenzene for 15 minutes.

8. Bake in 70° C oven for 10 minutes (aids photoresist).

9. Develop photoresist for 60 seconds. (1:5;AZ 351:DI water)

10. Pre-metal clean --- 20 sec (1:20;NH_4OH:DI water). Etches photoresist from gate region.

11. Rinse with DI water, blow dry with nitrogen.

12. Place wafer in evaporation chamber.

13. Load metal pellets.

14. Lower bell jar insuring seal is good.

15. Lower pressure to 10^{-6} torr.

16. Metal is evaporated automatically.

17. Remove wafer from chamber.

18. Liftoff metal with acetone soak: 5-10 minutes using ultrasonic tank occasionally.

19. Strip photoresist and blow dry with nitrogen.

Removal of p+ Layer

1. Prepare a PH 7.05 solution in the following manner:

   a) Place 30 ml of Hydrogen Peroxide in a 100 ml beaker.

   b) In a separate 100 ml beaker pour 10 ml of Ammonium Hydroxide and fill the beaker with DI water, stir and then pour all but 20ml out. Fill beaker again with DI water and stir.

2. Place pH probe into beaker with hydrogen peroxide. While stirring constantly, using an eyedropper put the dilute ammonium hydroxide solution into the hydrogen peroxide a few drops at a time. When the pH is 7.05 and steady, the etch is prepared. Stirring insures that the pH will change at a moderate rate.

3. The pH 7.05 etch is GaAs selective, with a 1000 Å/min etch rate. For typical p+ layers (75-100)Å a 6-7 sec etch time is satisfactory.

4. Dip the wafer into the pH 7.05 etch for the required time.

5. Immediately rinse with DI water and blow dry with nitrogen.

6. The fabrication process is now complete.

APPENDIX D

Transistor Characteristics

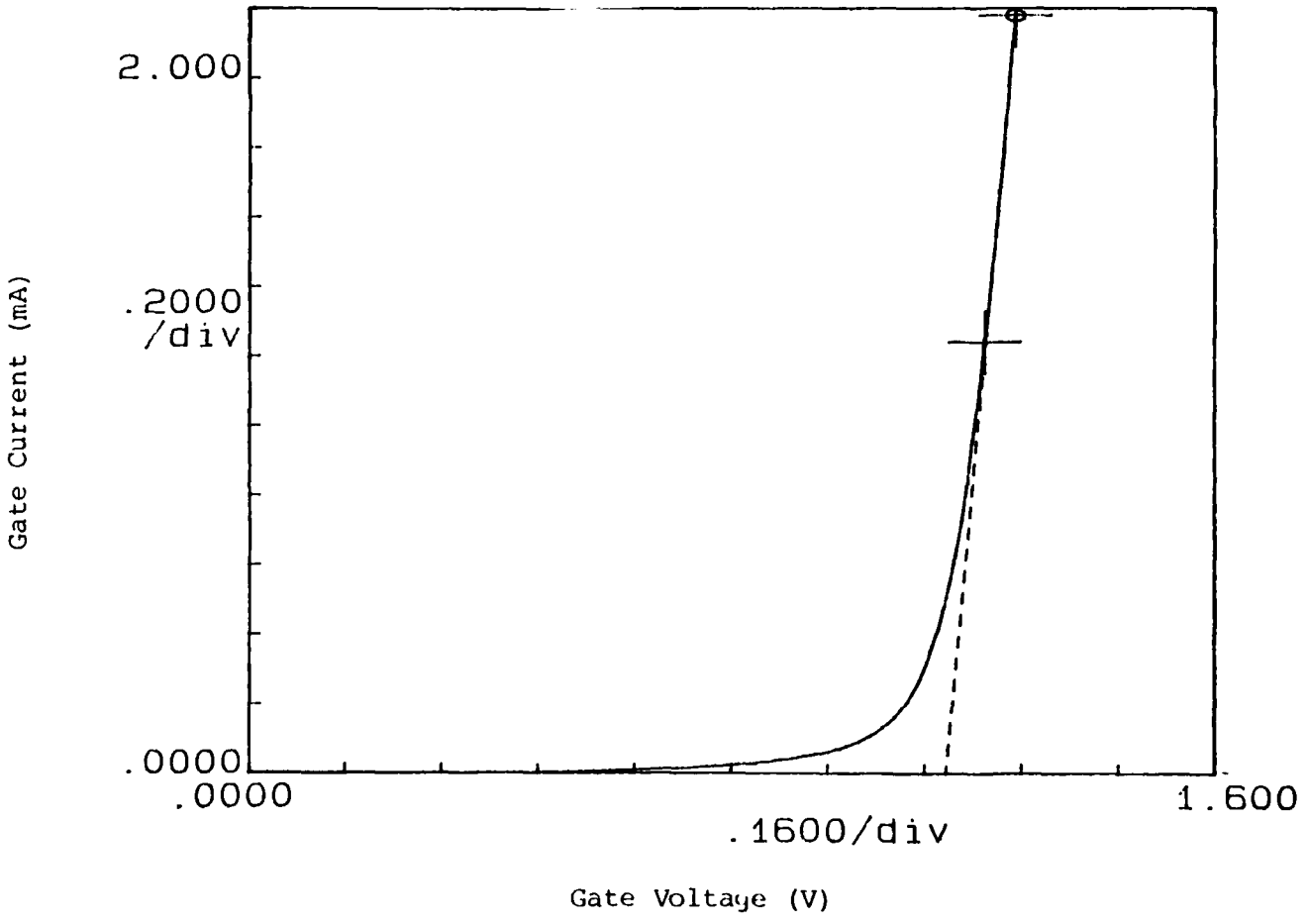


Fig D-1 Gate I-V for Sample 2263

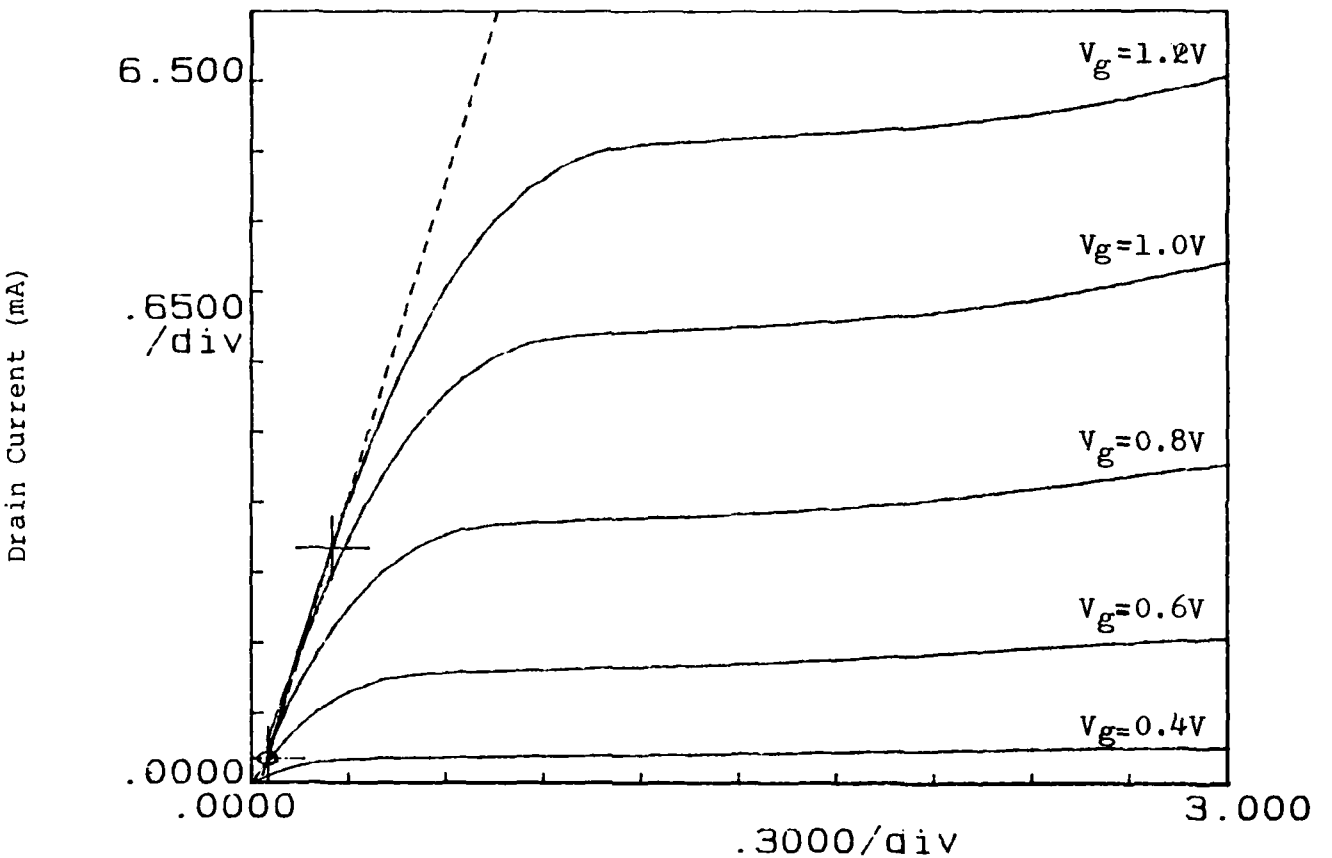


Fig D-2 Drain I-V for Sample 2263

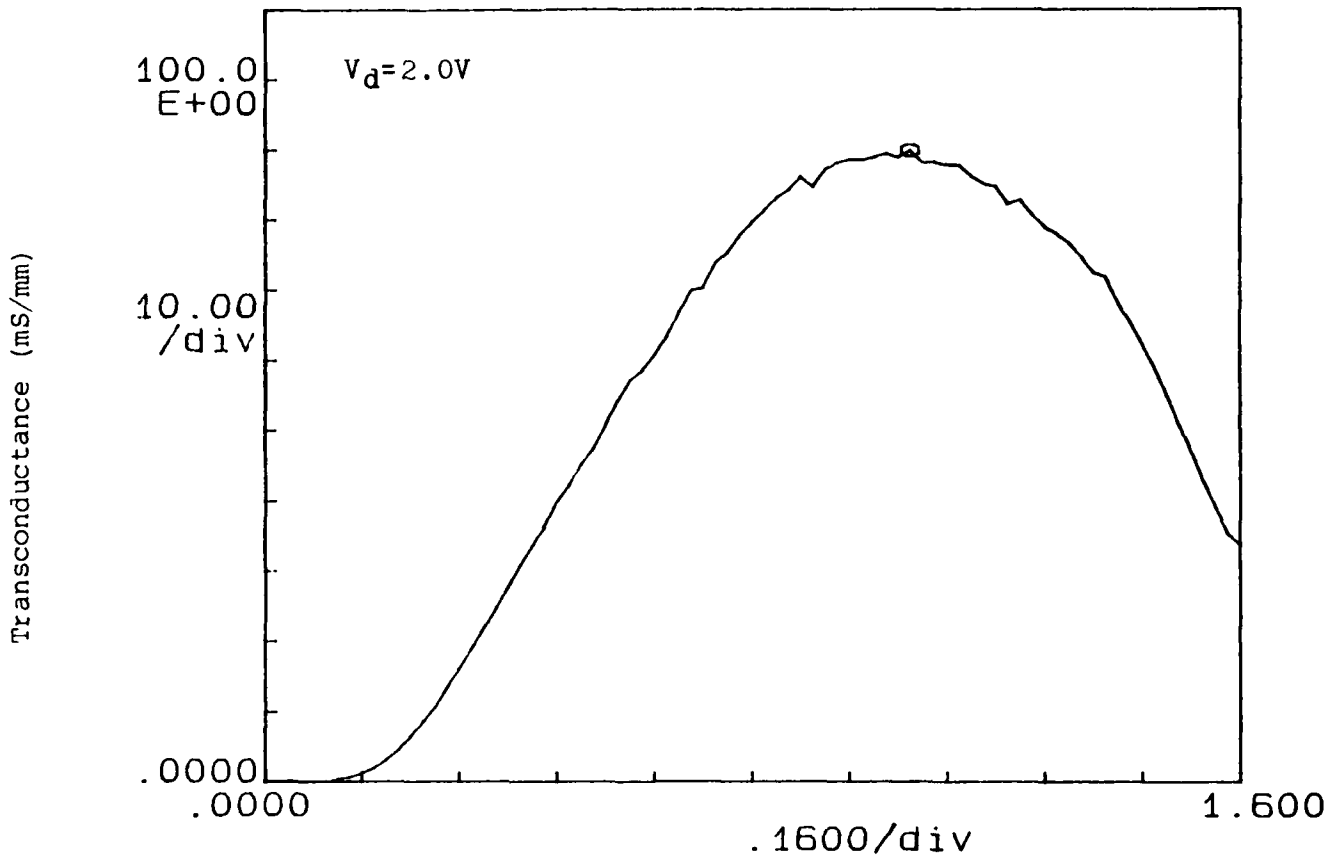


Fig D-3 Transconductance vs Gate Voltage for Sample 2263

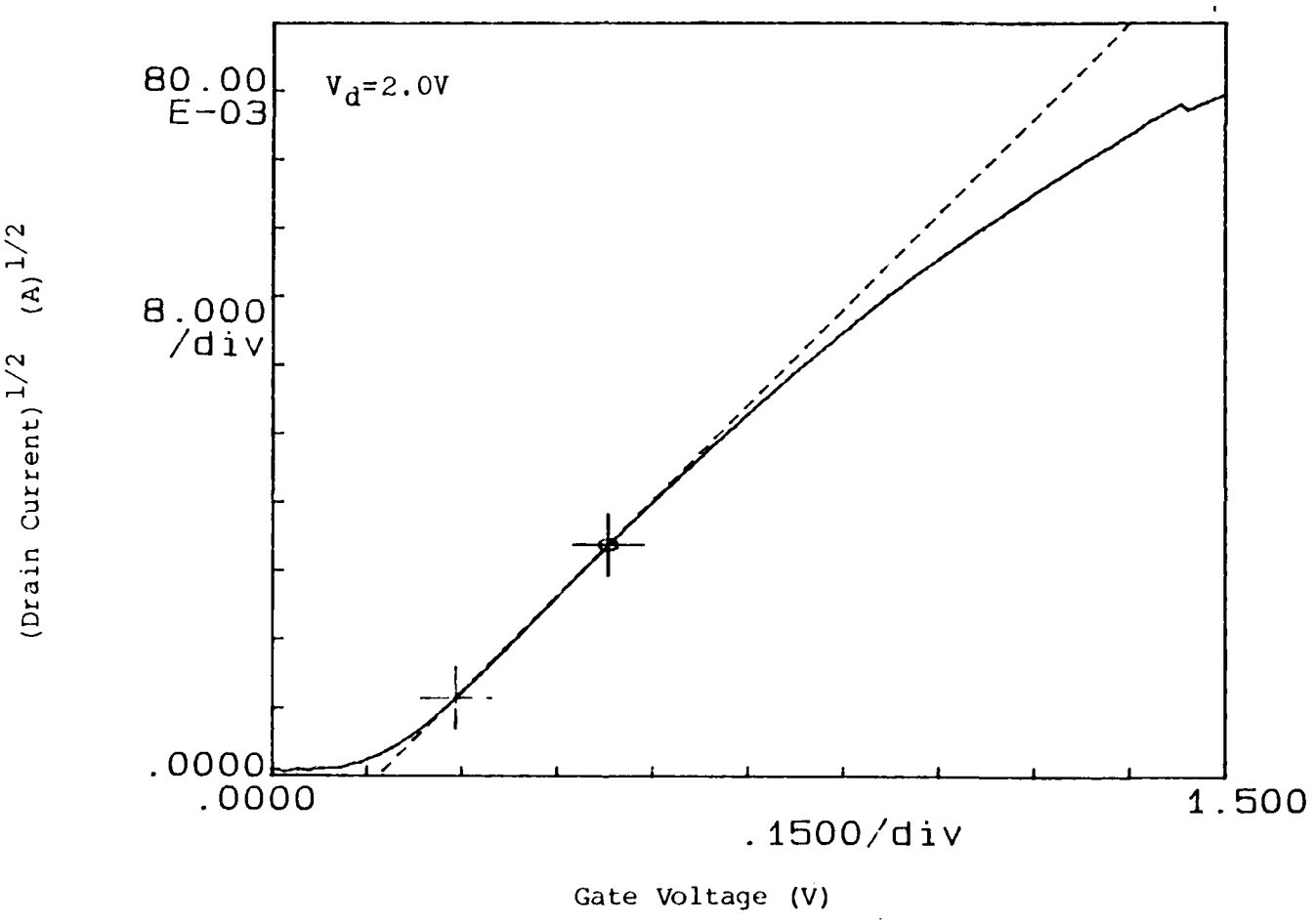


Fig D-4 I-V Curve Used to Determine V_{off} for Sample 2263

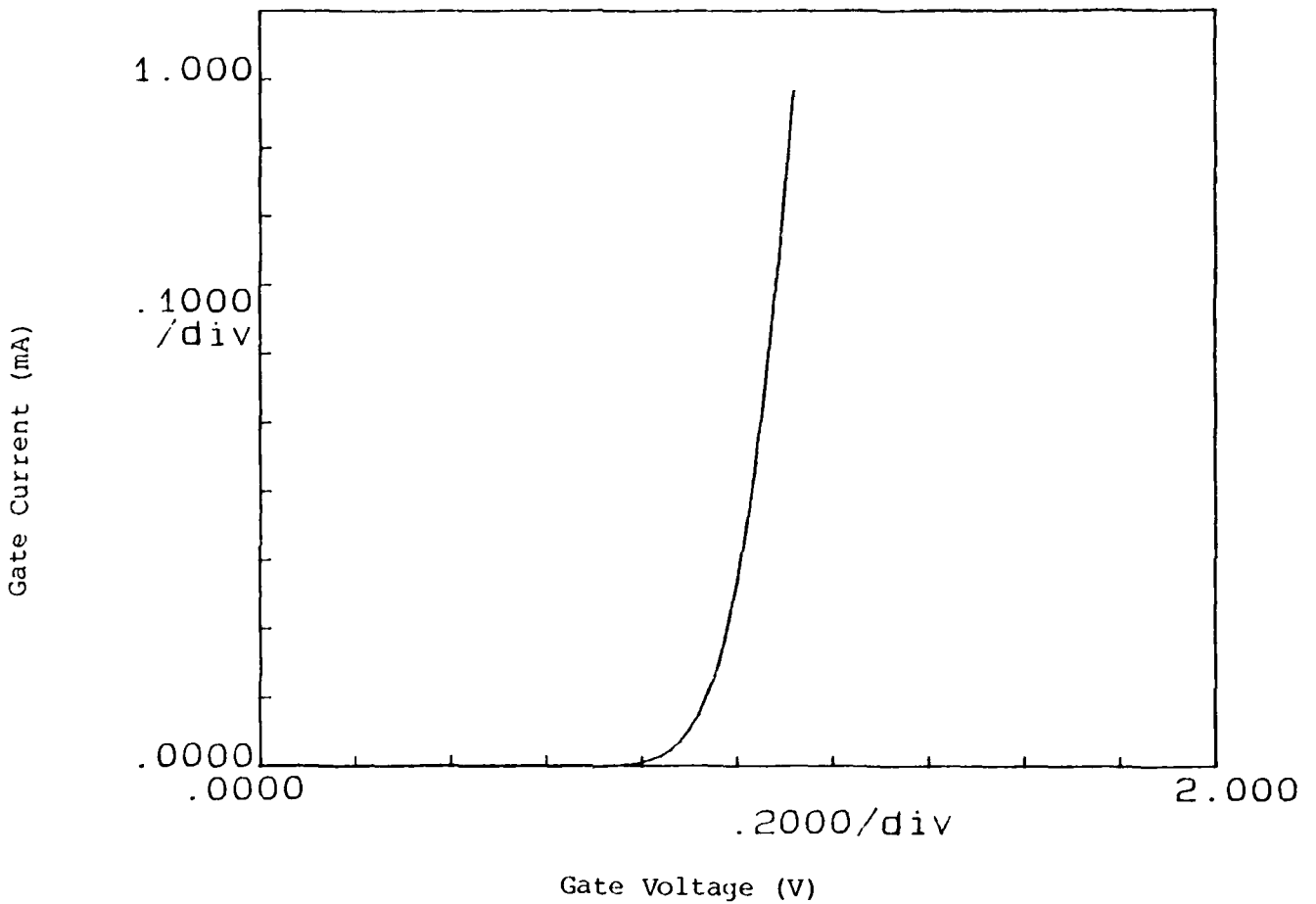


Fig D-5 Gate I-V for Sample 2265

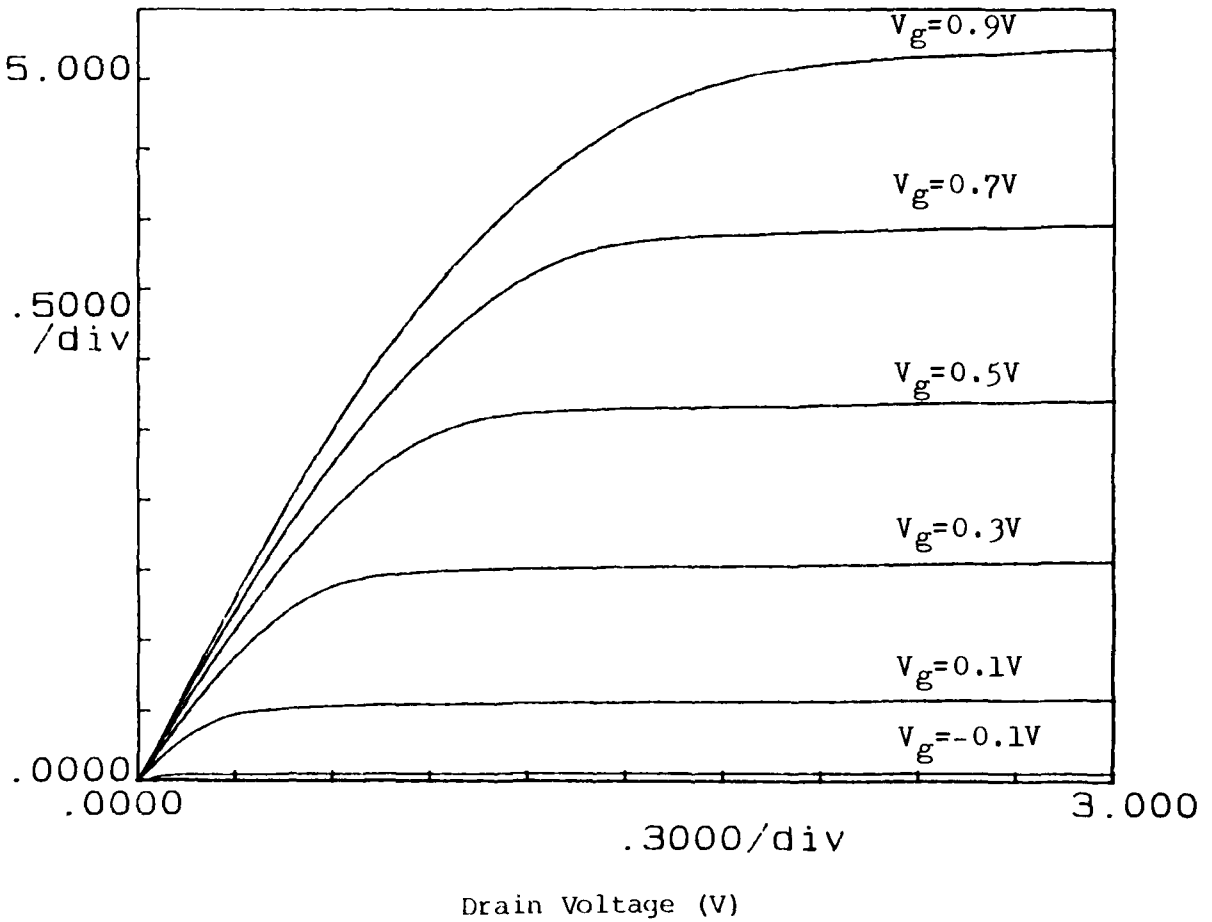


Fig D-6 Drain I-V for Sample 2265

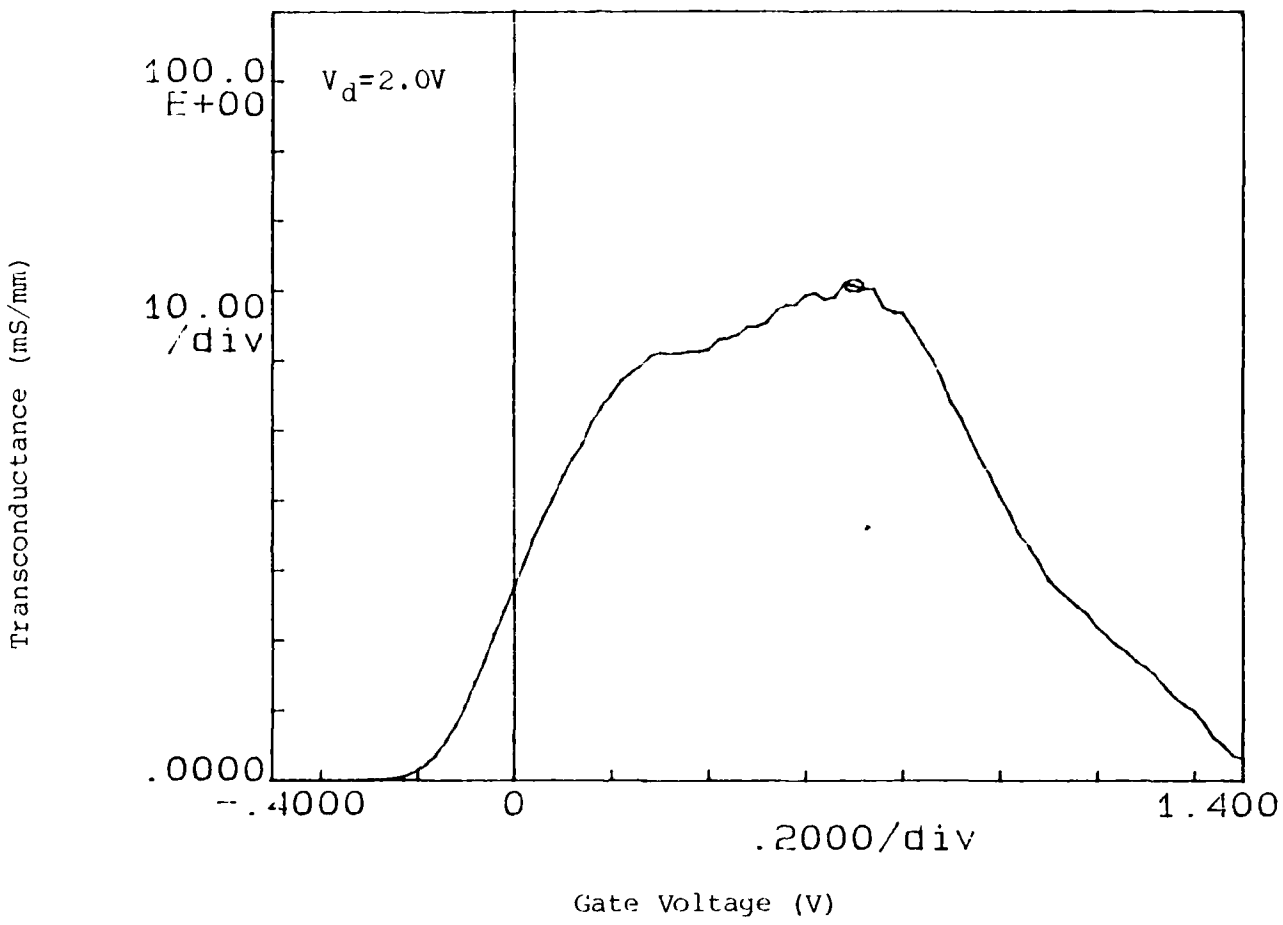


Fig D-7 Transconductance vs Gate Voltage for Sample 2265

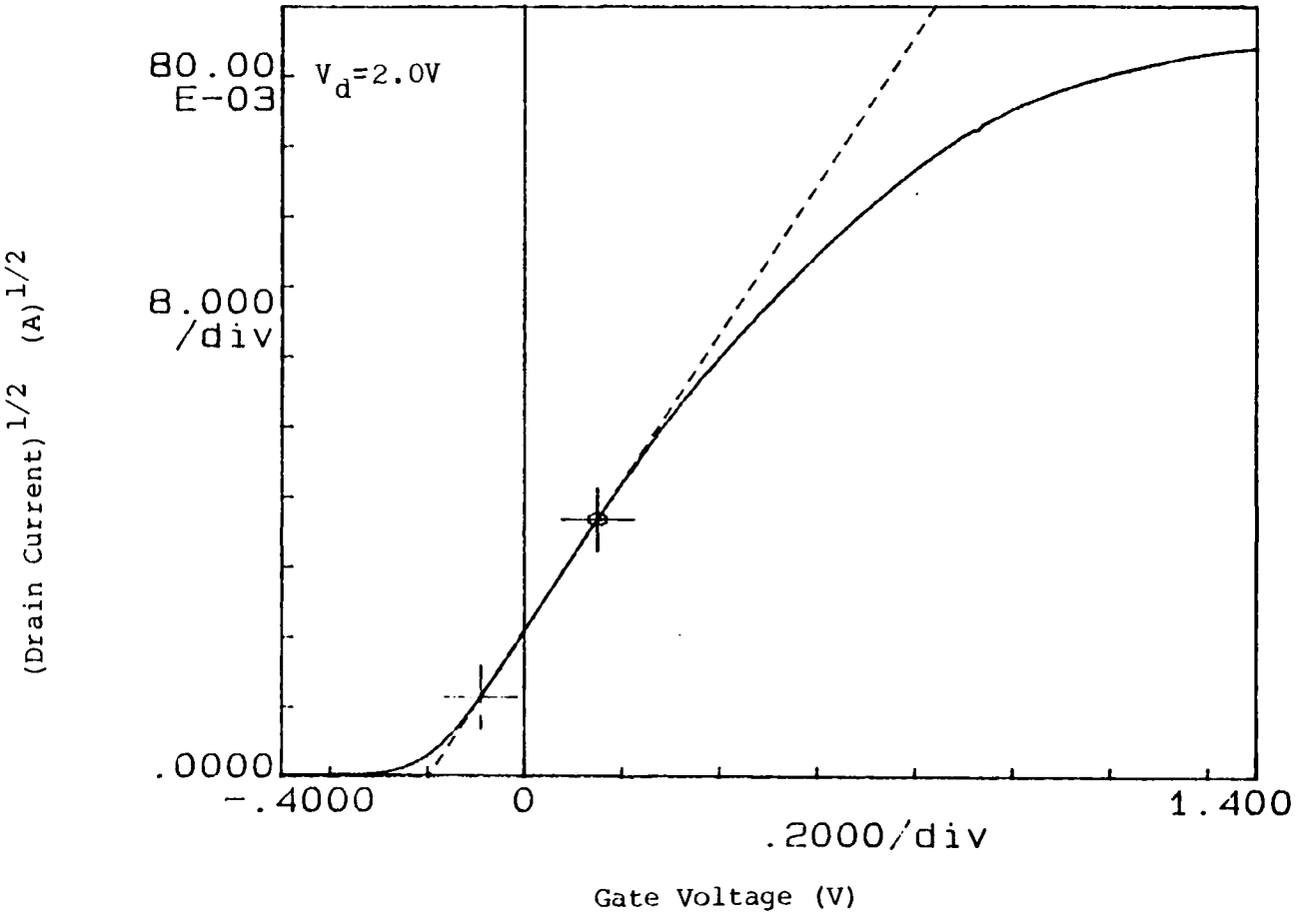


Fig D-8 I-V Curve Used to Determine V_{off} for Sample 2265

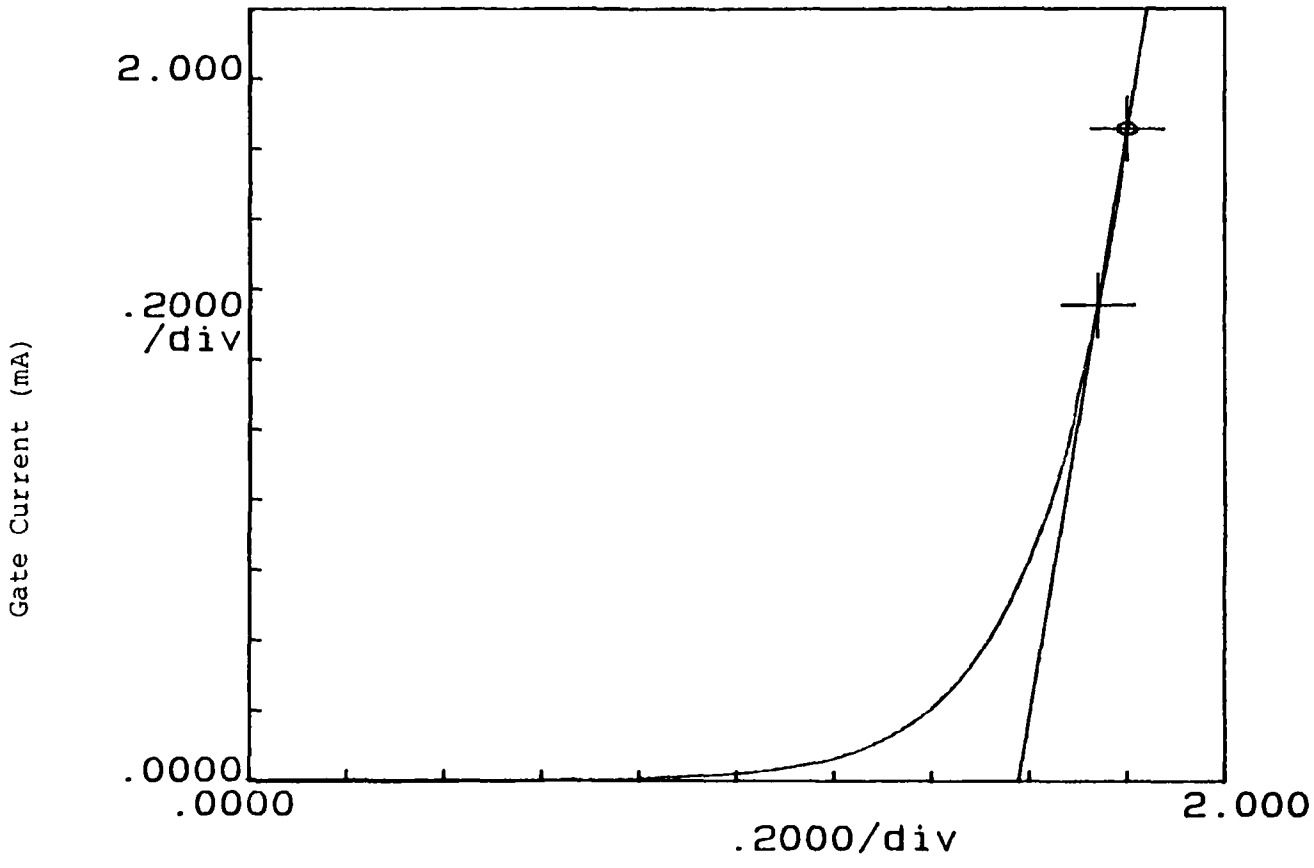


Fig D-9 Gate I-V for Sample 2373

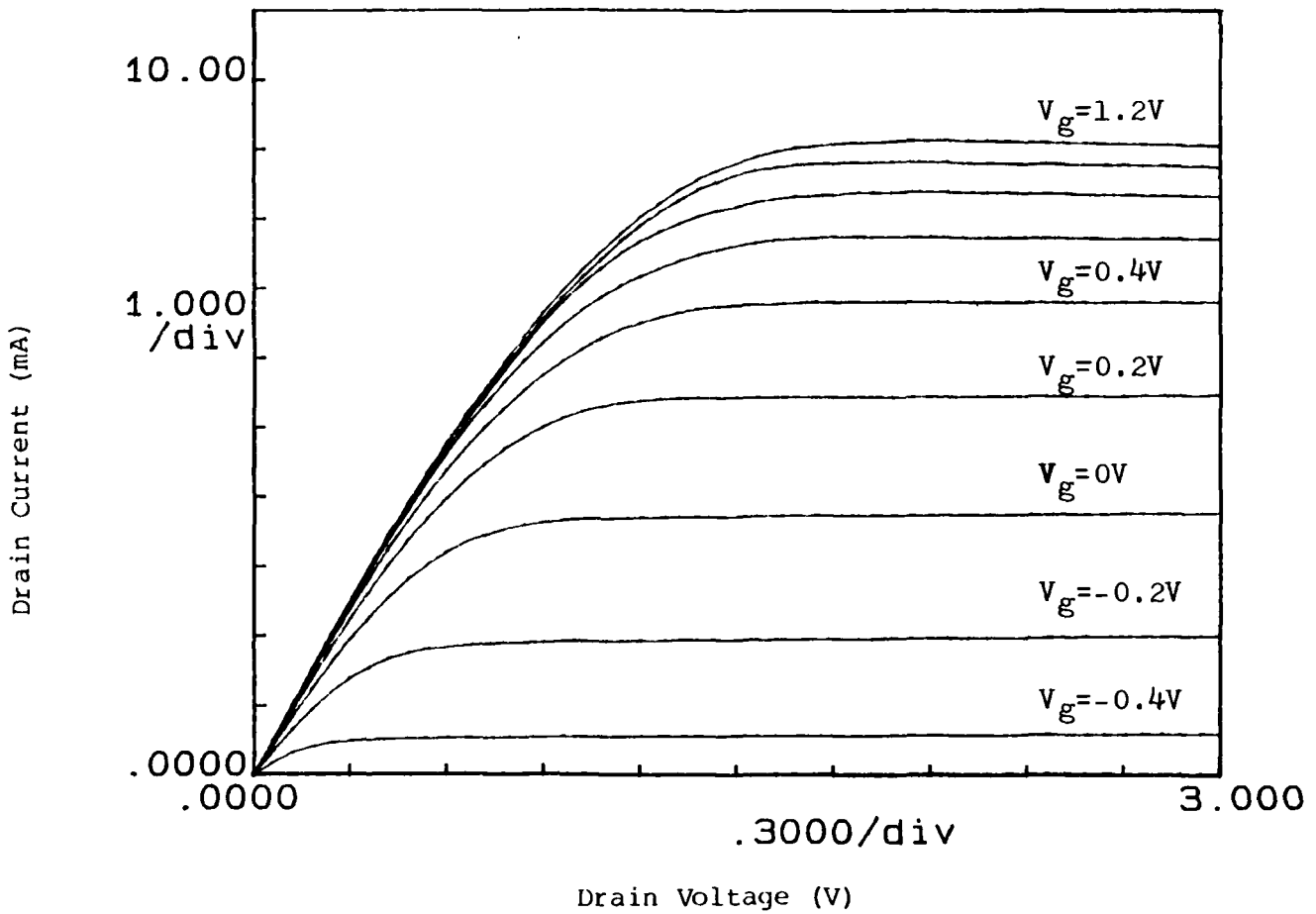


Fig D-10 Drain I-V for Sample 2373

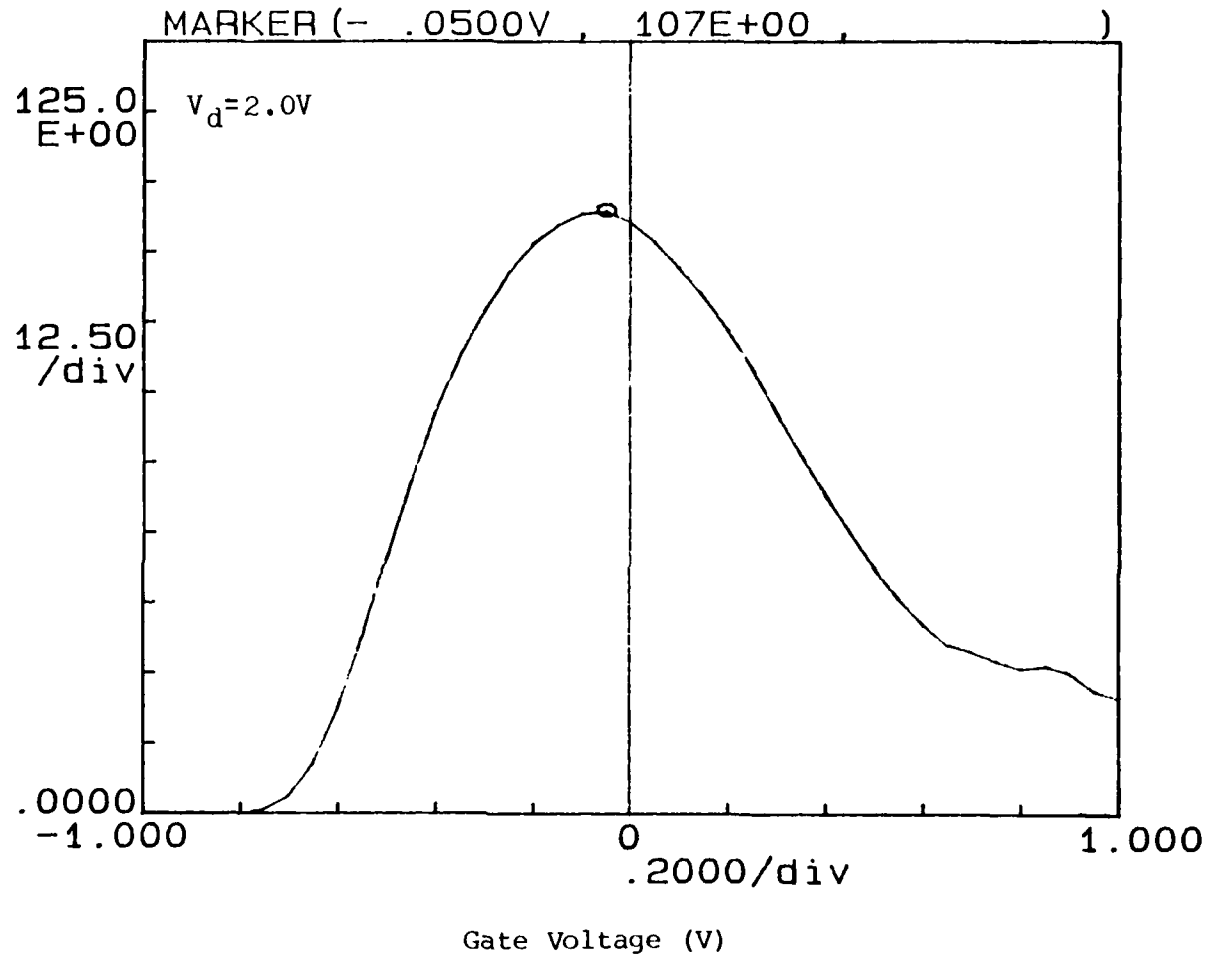


Fig D-11 Transconductance vs Gate Voltage for Sample 2373

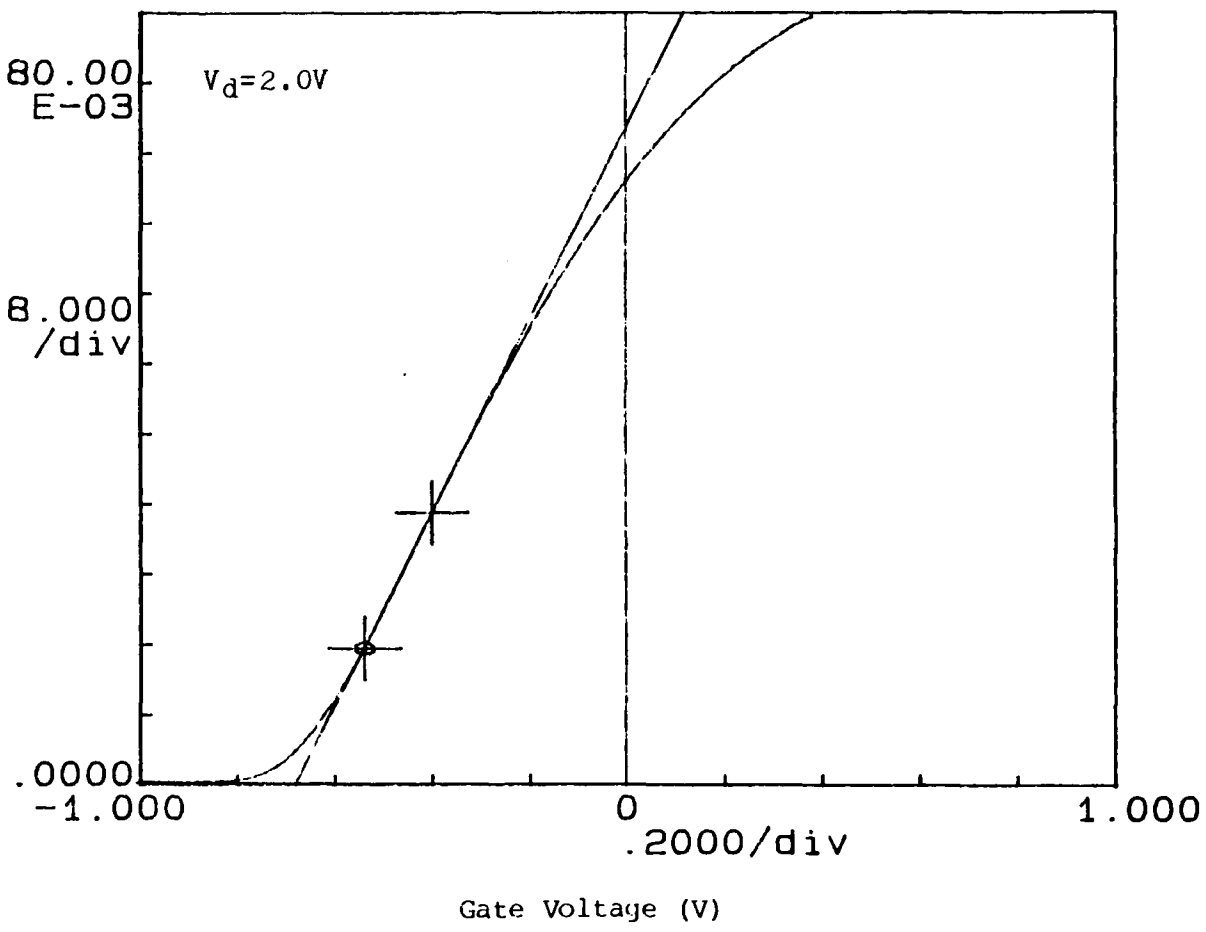


Fig D-12 I-V Curve Used to Determine V_{off} for Sample 2373

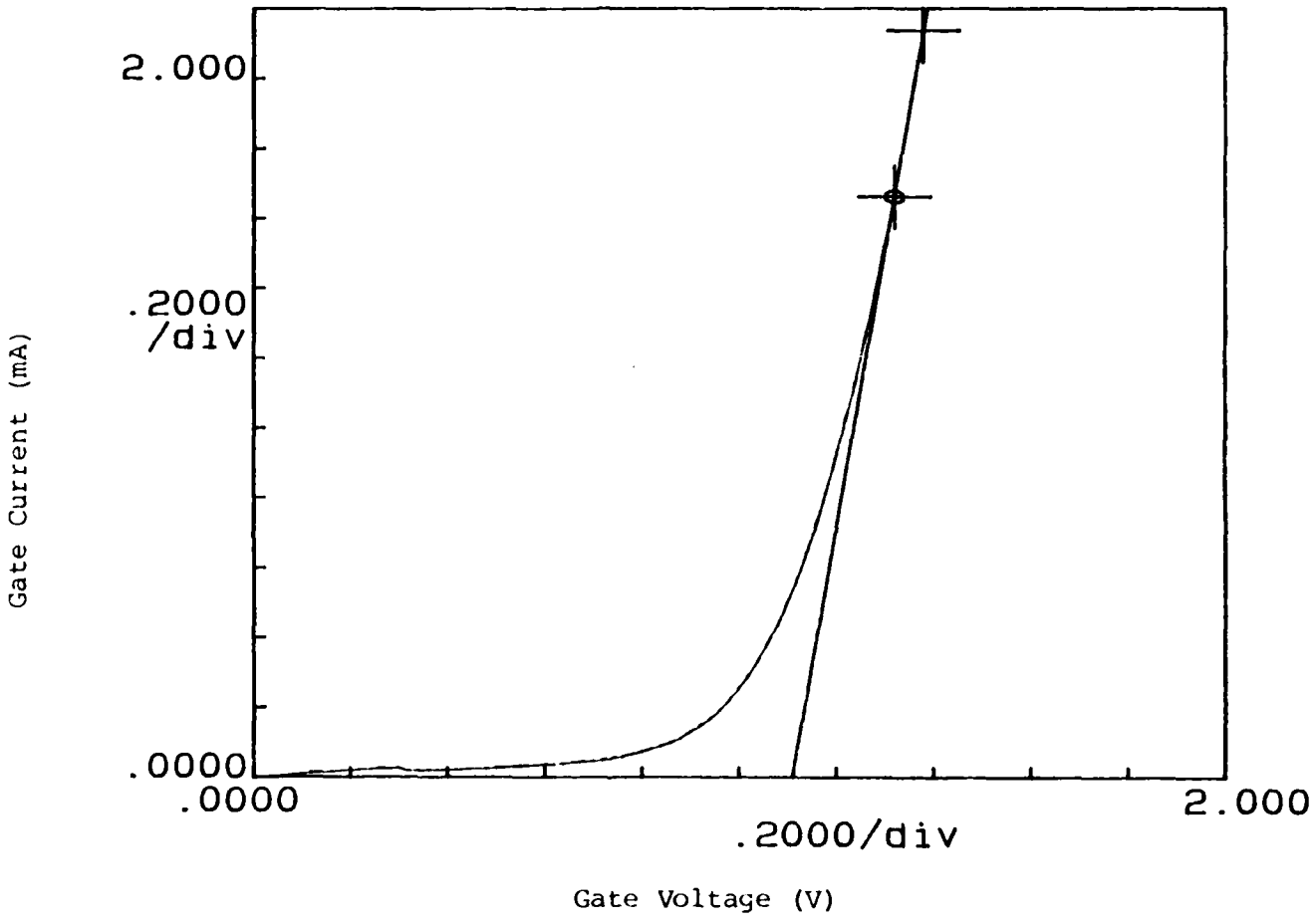


Fig D-13 Gate I-V for Sample 2376

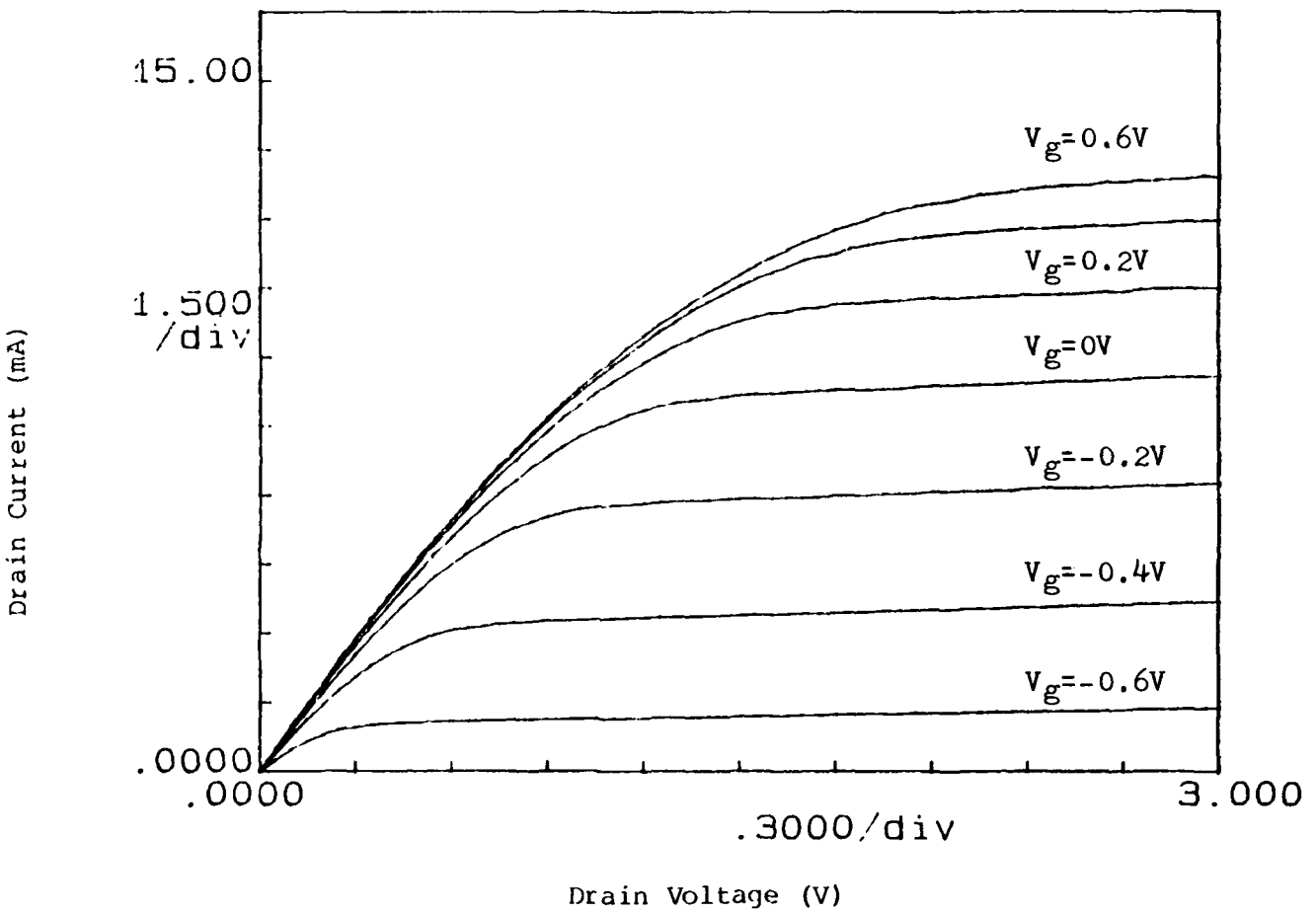


Fig D-14 Drain I-V for Sample 2376

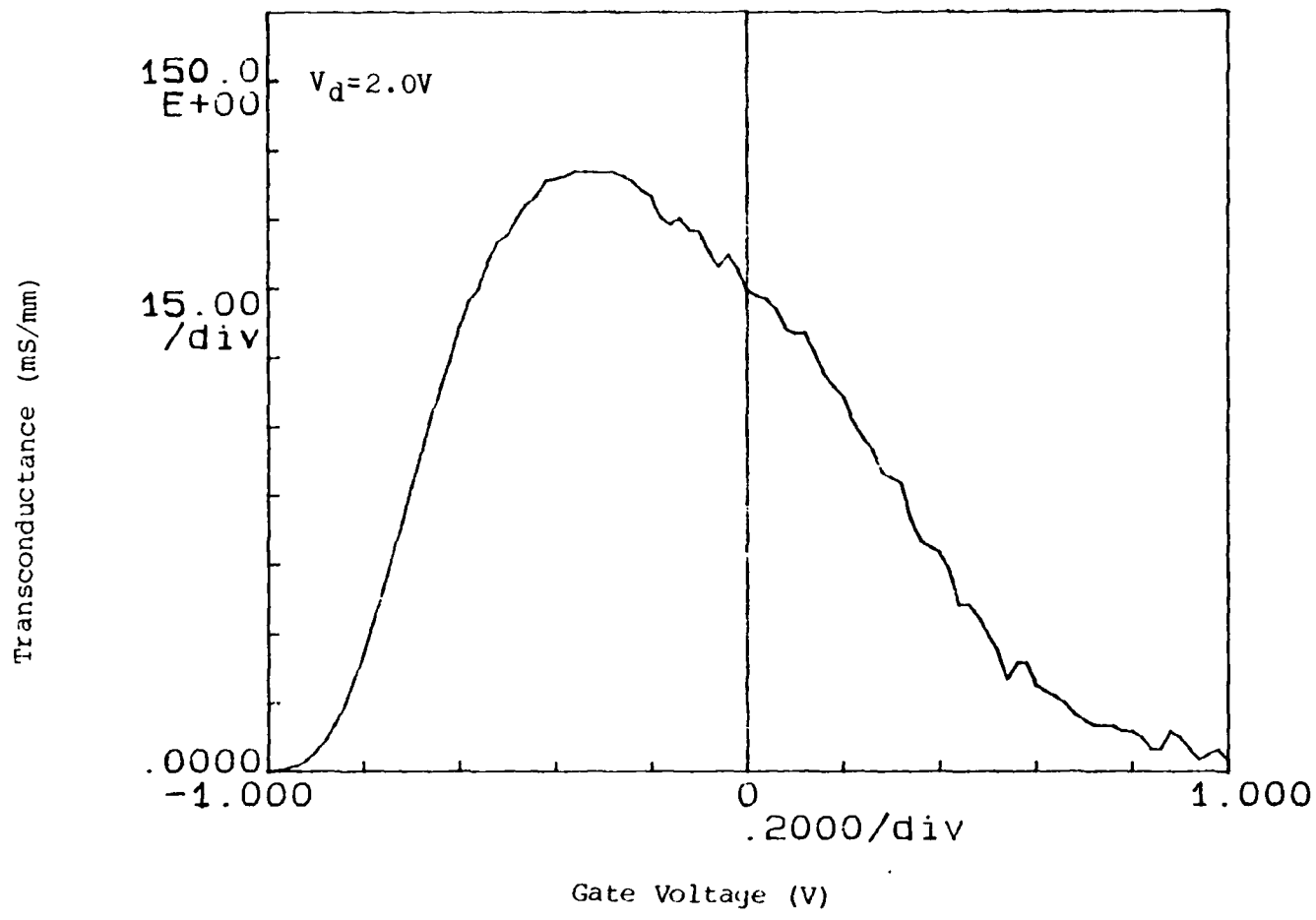


Fig D-15 Transconductance vs Gate Voltage for Sample 2376

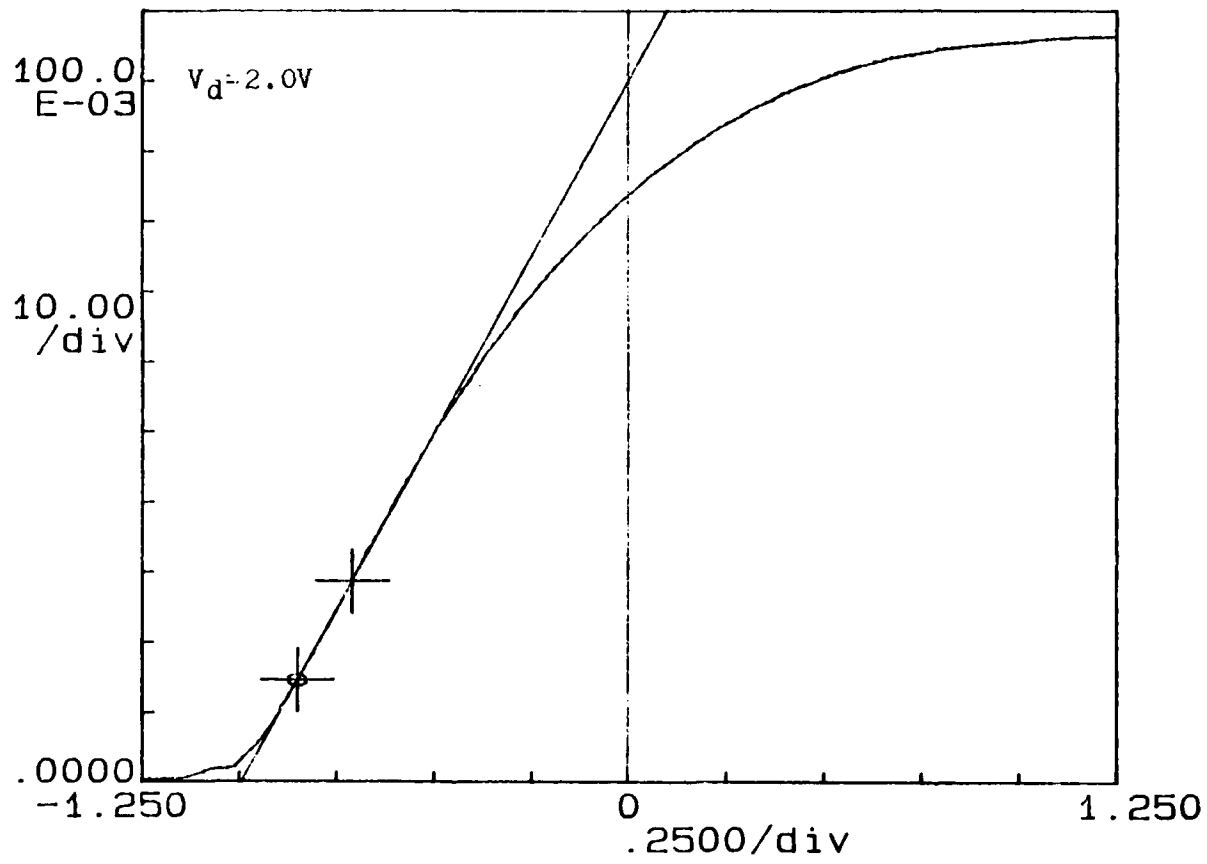


Fig D-16 I-V Curve Used to Determine V_{off} for Sample 2376

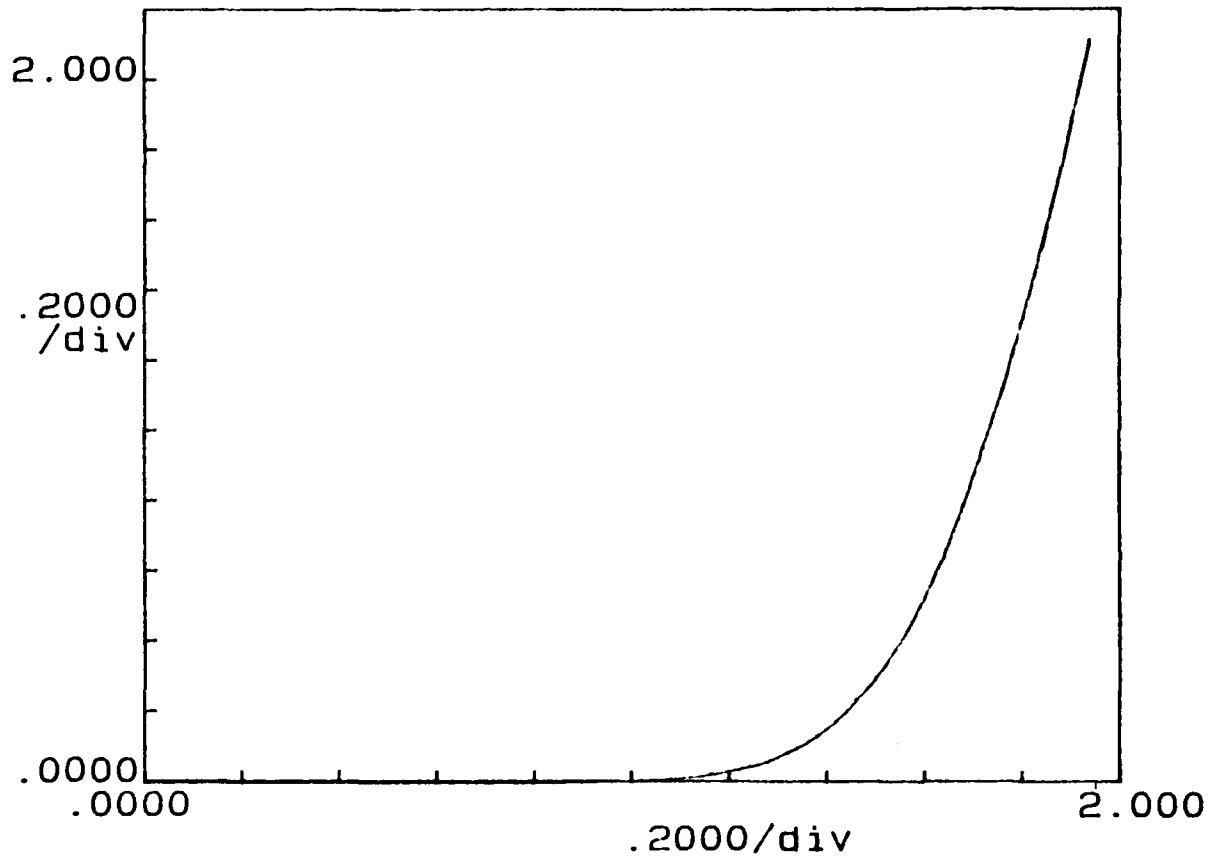


Fig D-17 Gate I-V for Sample 2377

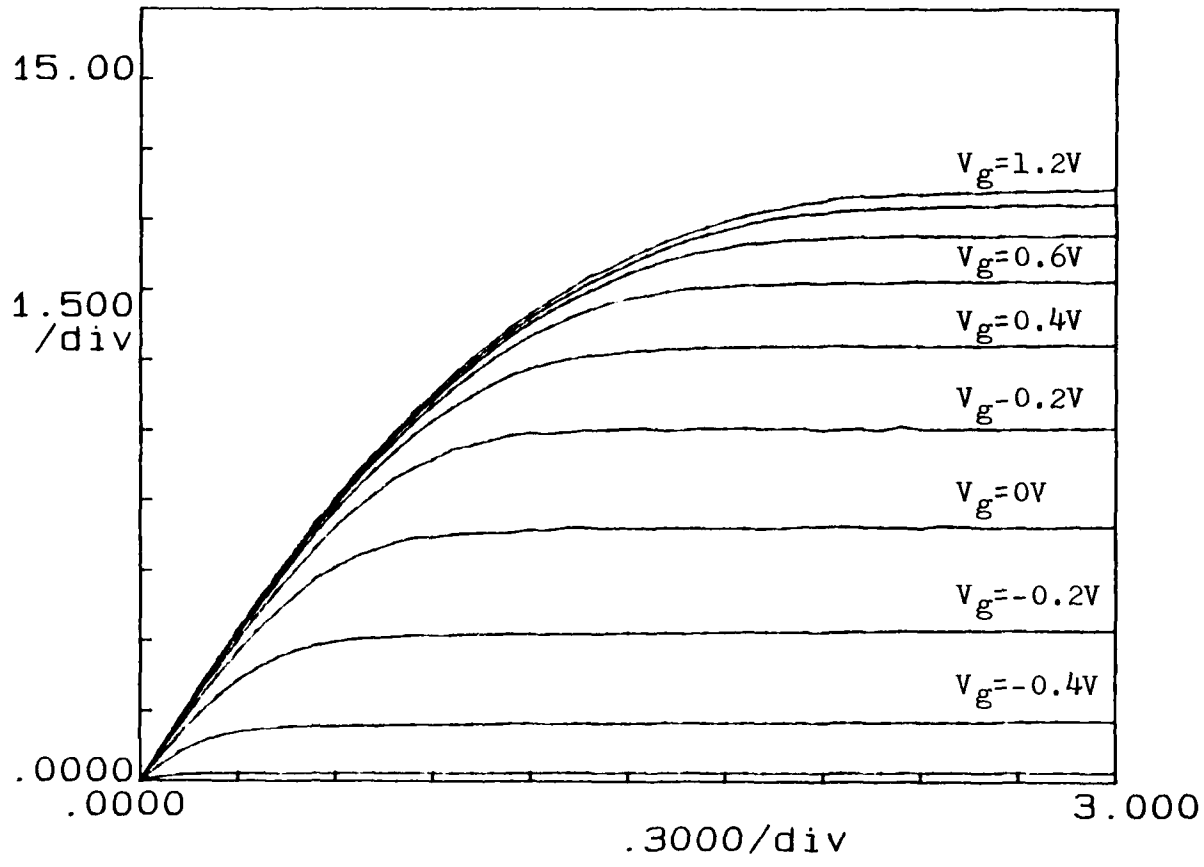


Fig D-18 Drain I-V for Sample 2377

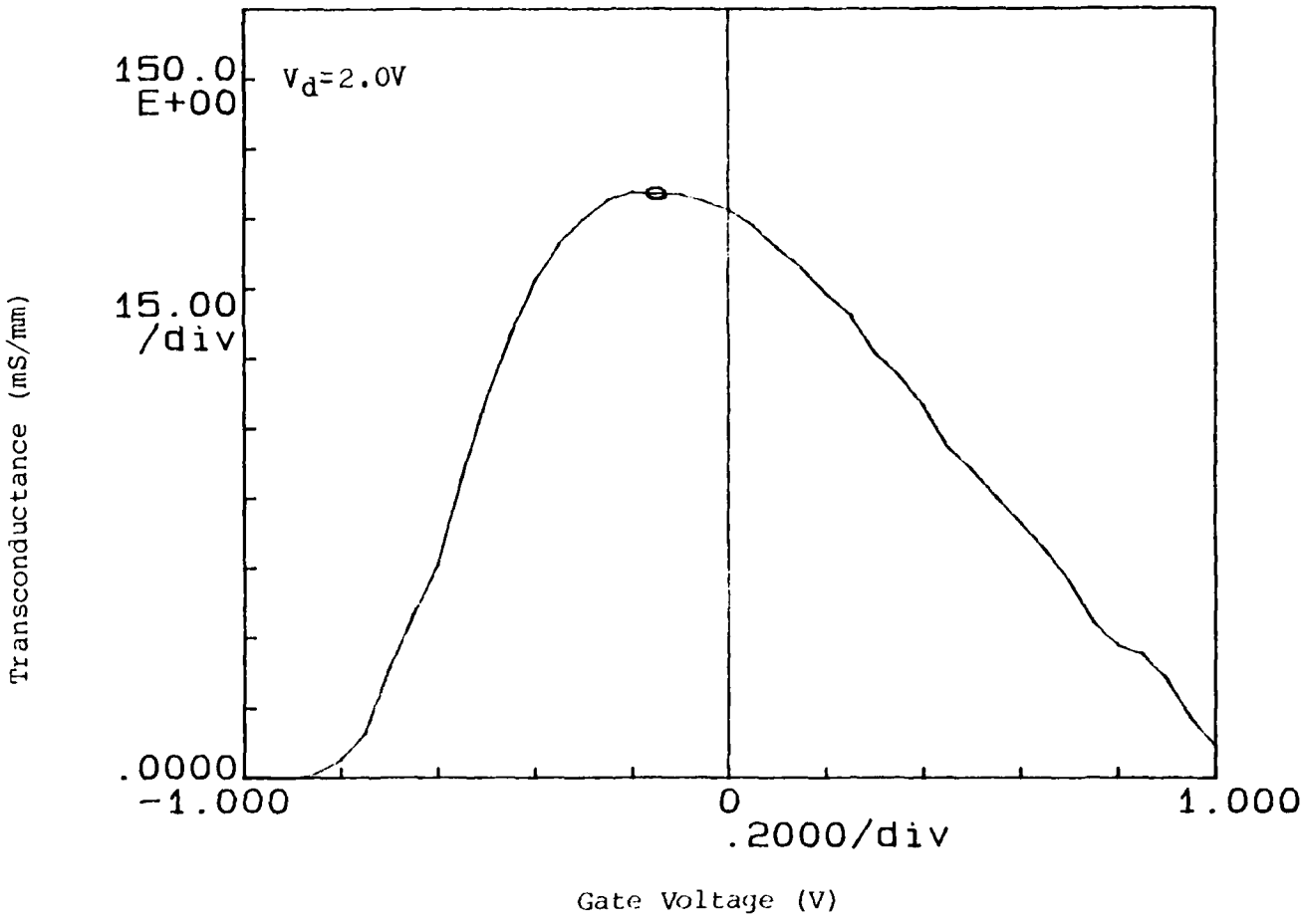


Fig D-19 Transconductance vs Gate Voltage for Sample 2377

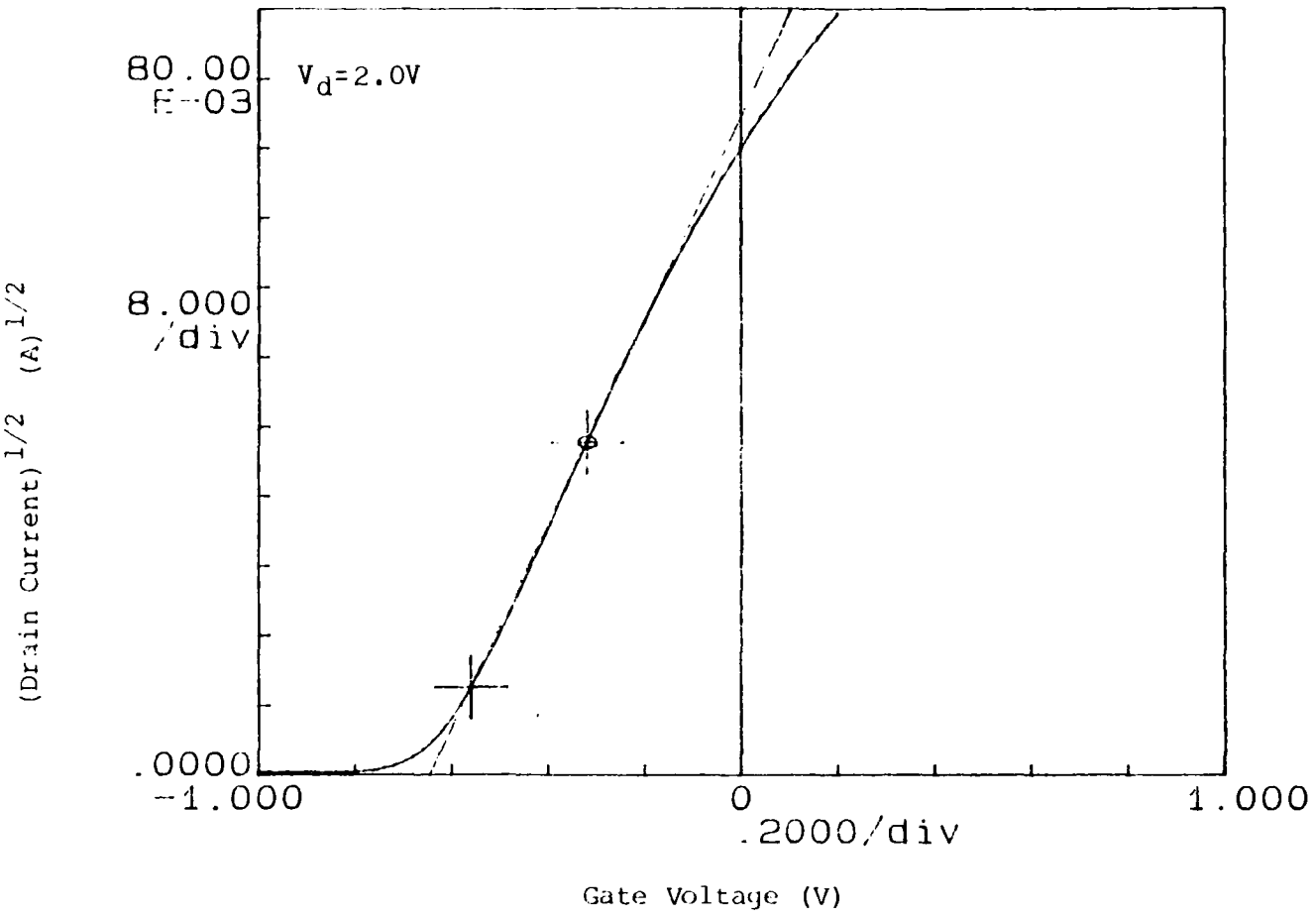


Fig D-20 I-V Curve Used to Determine V_{off} for Sample 2377

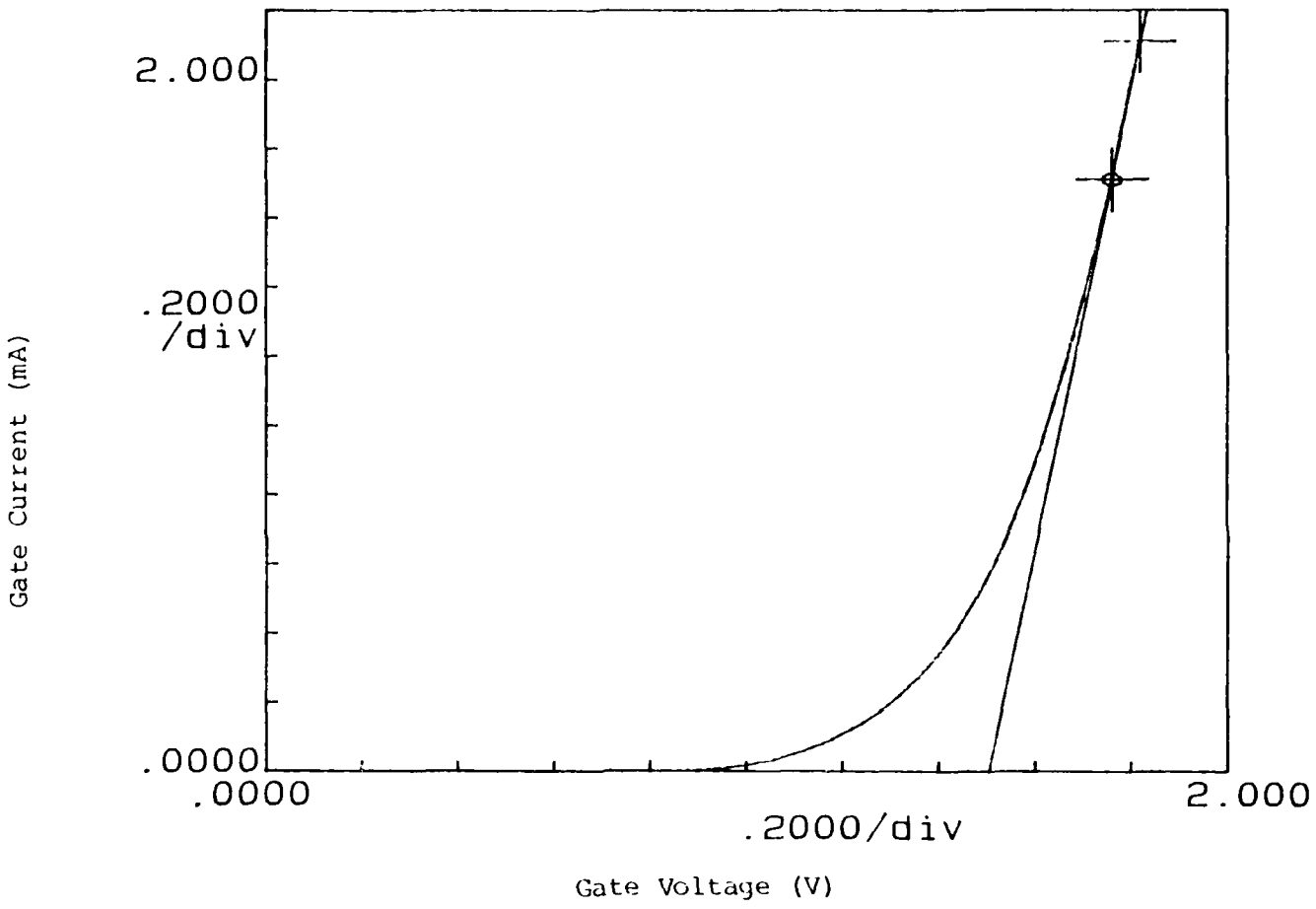


Fig D-21 Gate I-V for Sample 2378

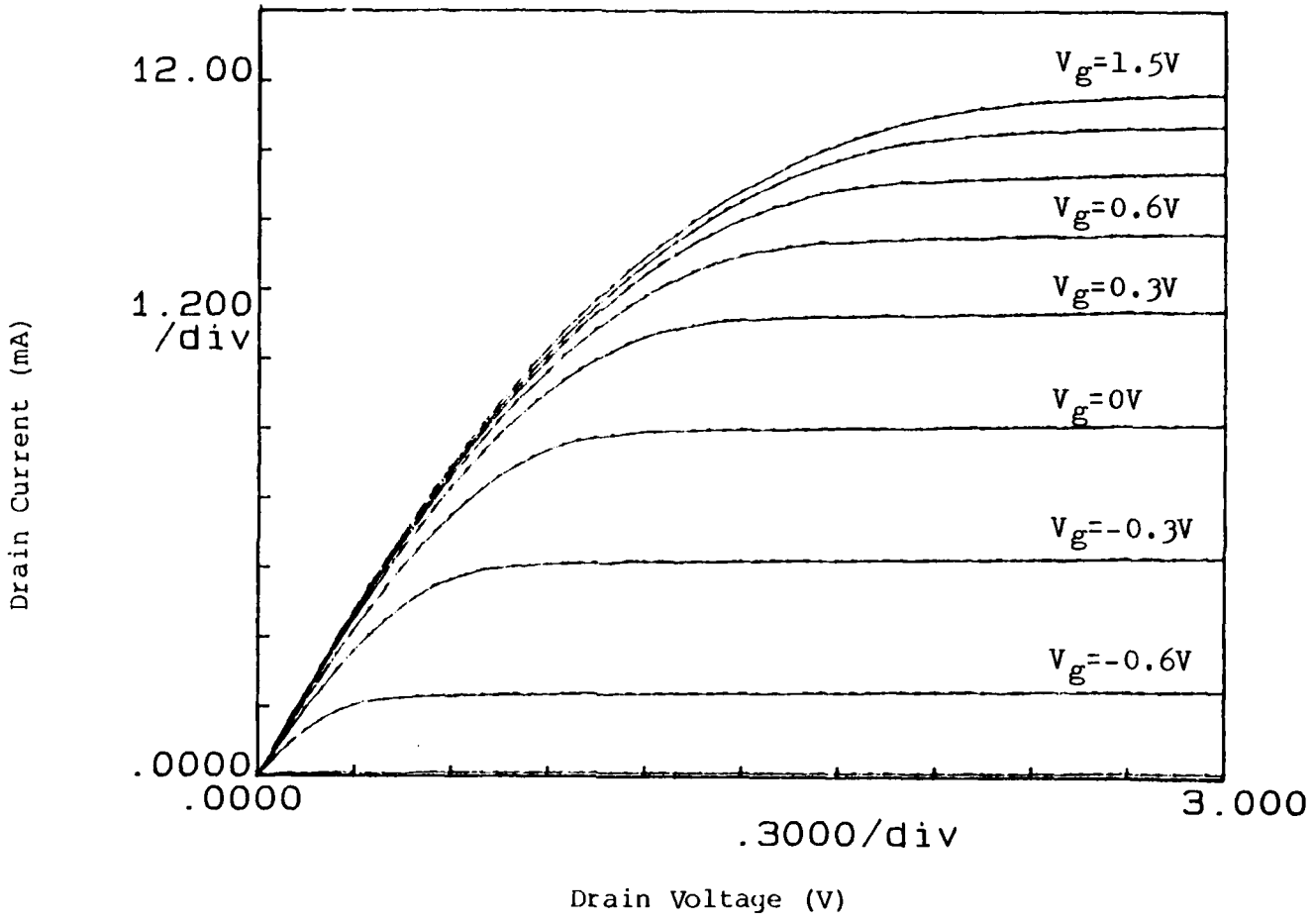


Fig D-22 Drain I-V Curve for Sample 2378

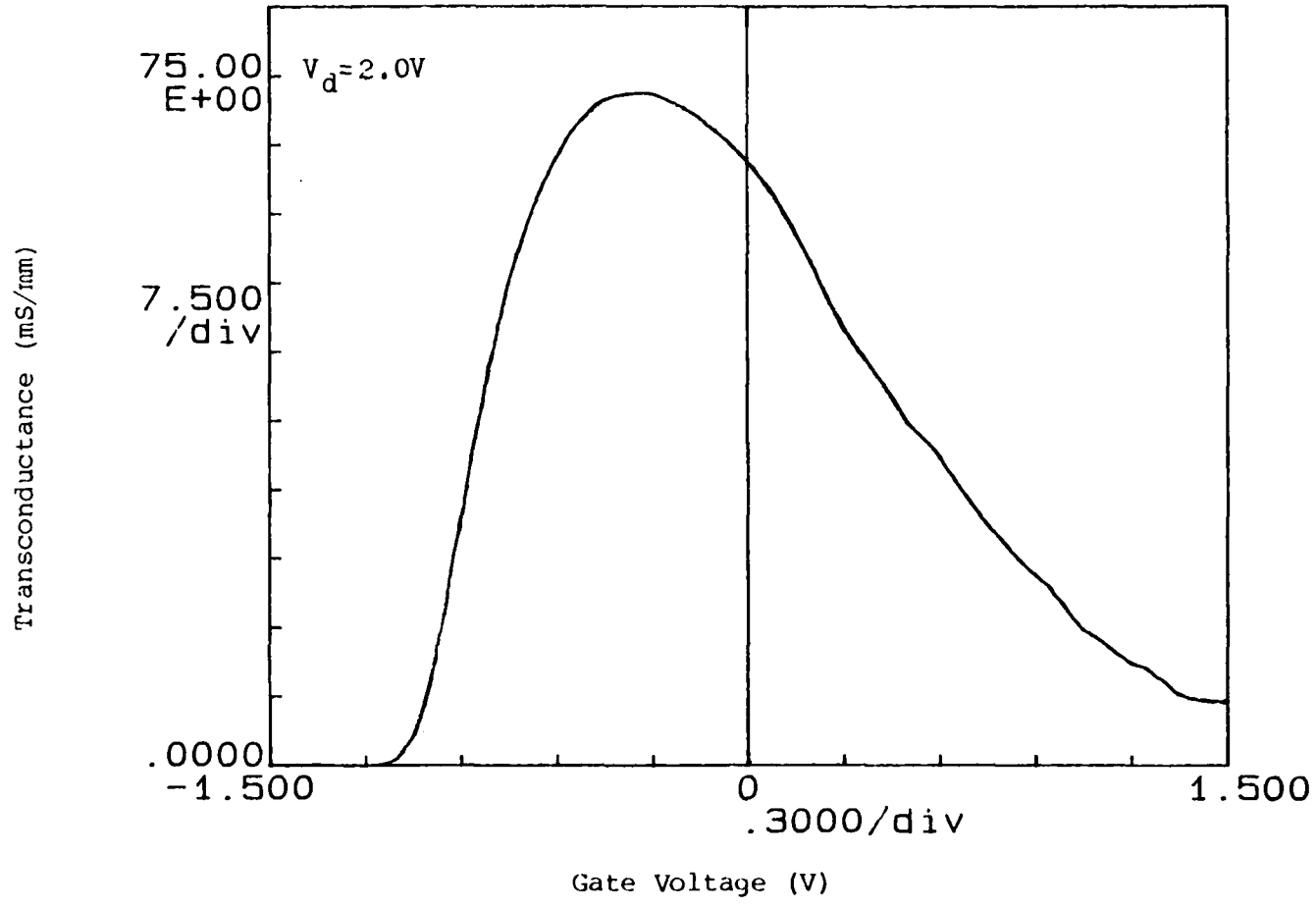


Fig D-23 Transconductance vs Gate Voltage for Sample 2378

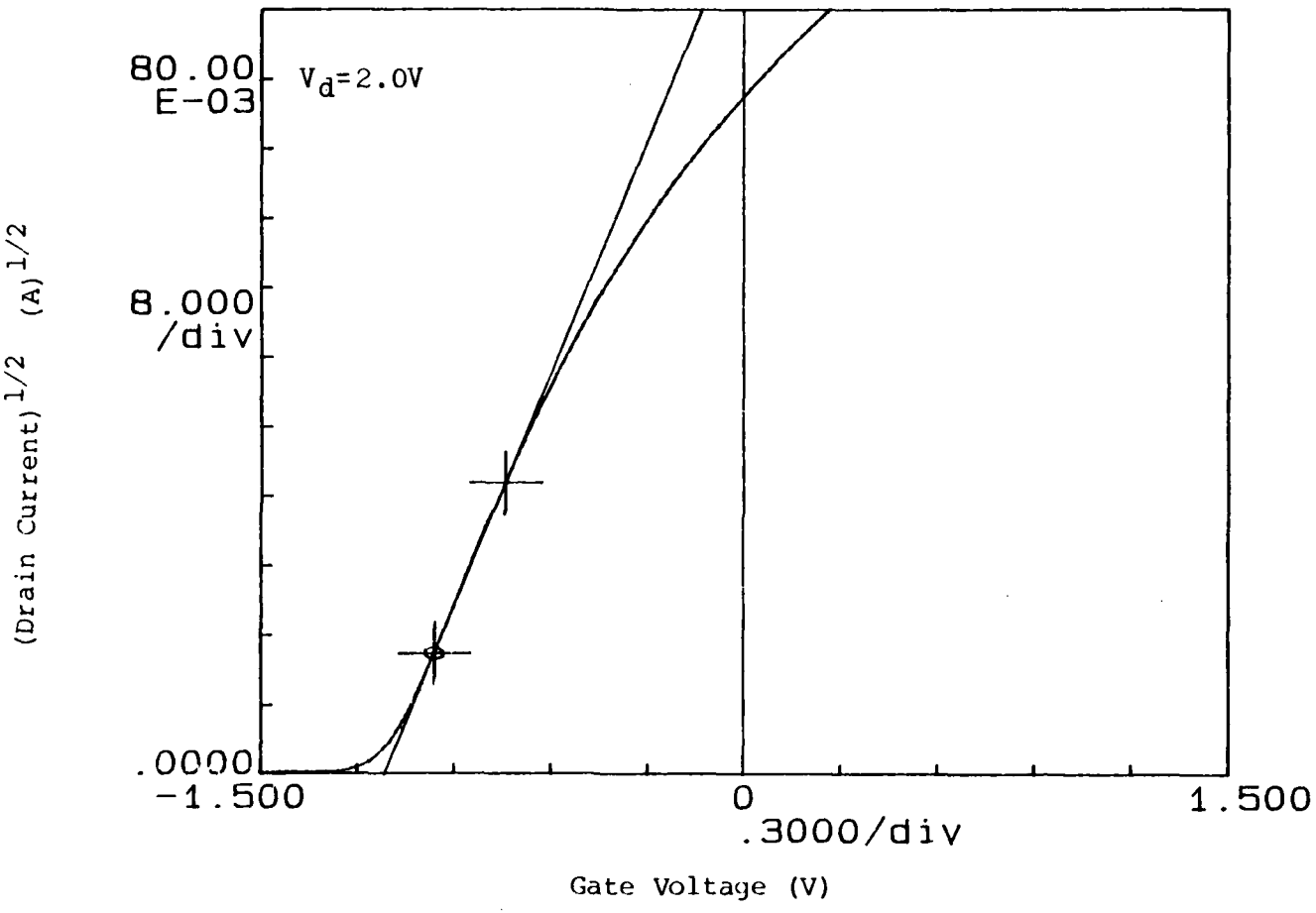


Fig D-24 I-V Curve Used to Determine V_{off} for Sample 2378

Bibliography

1. Aina, O., W. Katz, and B.J. Baliga. "Low-Temperature Sintered AuGe/GaAs Ohmic Contact," Journal of Applied Physics, 53:777-780 (January 1982).

2. Arnold, D., R. Fischer, W. Kopp, T. Henderson, and H. Morkoc. "Microwave Characterization of (AlGa)As/GaAs Modulation Doped FETs: Bias Dependence of Small Signal Parameters," IEEE Transactions on Electron Devices 31:1399-1402 (October 1984).

3. Brillson, L. J. "Contact Technology in III-V Device Analysis and Modification of Metal-Semiconductor Contact Interfaces in III-V Devices," Proceedings of the 1983 IEEE International Electron Device Meeting. 111-114. IEEE Press, New York, 1983.

4. Chand, N., T. Henderson, J. Klem, W. Masselink, and R. Fischer. "Comprehensive Analysis of Si-Doped $Al_xGa_{1-x}As$ (x=0 to 1):Theory and Experiments," Physical Review B 30:4481-4492 (15 October 1984).

5. Das, M., W. Kopp, and H. Morkoc. "Determination of Carrier Saturation Velocity in Short-Gate-Length Modulation Doped FET's," IEEE Electron Device Letters 31:446-449 (November 1984).

6. Delagebeaudeuf, D., P. Delescluse, M. Laviron, P. Tung, J. Chaplart, J. Chevrier, and N. Linh. "Low and High Field Transport Properties in Two-Dimensional Electron Gas FET," Institute of Physics Conference Ser. No. 65 Chapter 5:393-398, 1982.

7. Delagebeaudeuf,D. and N.T. Linh. "Metal-(n)AlGaAs-GaAs Two-Dimensional Electron Gas FET," IEEE Transactions on Electron Devices ED-29:955-960 (June 1982).

8. Delagebeaudeuf,D., M. Laviron, P. Delescluse, P. Tung, J. Chaplart, and N. Linh. "Planar Enhancement Mode Two Dimensional Electron Gas FET Associated with a Low AlGaAs Surface Potential," Electronics Letters 18:103-105 (21 January 1982).

9. Delagebeaudeuf, D. and N. Linh. "Charge Control of the Heterojunction Two-Dimensional Electron Gas for MESFET Application," IEEE Transactions on Electron Devices ED-28:790-794 (July 1981).

10. Drummond, T., S. Su, W. Kopp, R. Fischer, R. Thorne and H. Morkoc. "High Velocity N-On and N-Off Modulation Doped GaAs/$Al_xGa_{1-x}As$ FETs," Proceedings of the 1982 International Electron Devices Meeting. 586-589. IEEE Press, New York, 1982.

11. Drummond, T., W. Kopp, H. Morkoc, and M. Keever. "Transport in Modulation Doped Structures ($Al_xGa_{1-x}As$/GaAs) and Correlation with Monte Carlo Calculations (GaAs)," Applied Physics Letters 41(3):277 (1 August 1982).

12. Drummond, T., W. Kopp, R. Thorne, R. Fischer, and H. Morkoc "Influence of $Al_xGa_{1-x}As$ Buffer Layers on the Performance of Modulation Doped Field-Effect Transistors," Applied Physics Letters 40:879-881 (15 May 1982).

13. Drummond, T., W. Kopp, M. Keever, H. Morkoc, and A. Cho. "Electron Mobility in Single and Multiple Period Modulation-Doped (Al,Ga)As/GaAs Heterostructures," Journal of Applied Physics 53:1023-1027 (February 1982).

14. Drummond, T., W. Kopp, R. Fischer, and H. Morkoc. "Influence of AlAs Mole Fraction on the Electron Mobility of (Al,Ga)As/GaAs Heterostructures," Journal of Applied Physics 53:1028-1029 (February 1982).

15. Drummond, T., H. Morkoc, K. Hess, and A. Cho. "Experimental and Theoretical Electron Mobility of Modulation Doped $Al_xGa_{1-x}As$/GaAs Heterostructures Grown By Molecular Beam Epitaxy," Journal of Applied Physics 52:5231-5234 (August 1981).

16. Drummond, T., H. Morkoc, and A. Cho. "Dependence of Electron Mobility on Spatial Separation of Electrons and Donors in $Al_xGa_{1-x}As$/GaAs Heterostructures," Journal of Applied Physics 52:1380-1386 (March 1981).

17. Eglash, S., N. Newman, S. Pan, W. Spicer, D. Collins, and M. Zurakowski. "Barrier Heights From Ohmic to Bandgap: Modified Al:GaAs Schottky Diodes by MBE," Proceedings of the 1983 International Electron Devices Meeting. 119-122. IEEE Press, New York, 1983.

18. Feuer, M., R. Hendel, R. Kiehl, J. Hwang, V. Keramidas, C. Allyn, and R. Dingle. "High-Speed Low-Voltage Ring Oscillators Based on Selectively Doped Heterojunction Transistors," IEEE Electron Device Letters EDL-4:306-307 (September 1983).

19. Fischer, R., C. Hopkins, C. Evans, Jr., T. Drummond, W. Lyons, J. Klem, C. Colvard, and H. Morkoc. "The Properties of Si in MBE Grown AlGaAs," Institute of Physics Conference Ser. No. 65 Chapter 3:157-164, 1982.

20. Garner, C., C. Su, W. Saperstein, K. Jew, C. Lee, G. Pearson, and W. Spicer. "Effect of GaAs or $Ga_xAl_{1-x}As$ Oxide Composition on Schottky-Barrier Behavior," Journal of Applied Physics 50:3376-3382 (May 1979).

21. Grzyb, J., Electronic Device Process Engineer. Electronic Research Branch, Electronic Technology Division, Air Force Avionics Laboratory. Personal interviews. Wright-Patterson AFB, OH 1 March through 15 October 1984.

22. Heiblum, M., M. Nathan, and E. Eizenberg. "Measuring Barrier Heights in GaAs-AlGaAs and Metal-AlGaAs," 43rd Annual IEEE Device Research Conference. To be published. (June 1985).

23. Heiblum, M., M. Nathan, and C. Chang "Characteristics of AuGeNi Ohmic Contacts to GaAs," Solid State Electronics 25:185-195 (March 1982).

24. Hiyamizu,S., K. Kondo, T. Fujii, J. Saito, T. Ishikawa, and S. Tatsuta "MBE-Grown GaAs-AlGaAs Heterostructures on SI GaAs Substrates: Applications to Optoelectronic Integrated Circuits and HEMT LSIs," Semi-Insulating III-V Materials. Cheshire England, Shiva Publishing Limited, 1984.

25. Iliadis, A., and K. Singer. "Metallurgical Behavior of Ni/Au-Ge Ohmic Contacts to GaAs," Solid State Communications 49:99-101 (January 1984).

26. Jaros, M. and H.L. Hartnagel. "An Understanding of Ohmic Contact Formation with Ge Doping of n-GaAs," Solid State Electronics, 18:1029-1030 (November 1975).

27. Kamei, H. and A. Sasaki. "Mobility Calculation of Two-Dimensional Electron Gas in GaAs/AlGaAs Heterostructure at 4.2 K," Electronics Letters 18:309-311 (1 April 1982).

28. Keever, M., T. Drummond, H. Morkoc, K. Hess, and B. Streetman. "Hall Effect and Mobility in Heterojunction Layers," Journal of Applied Physics 53:1034-1036 (February 1982).

29. Ketterson, A., M. Moloney, and H. Morkoc. "Modeling of GaAs/AlGaAs MODFET Inverters and Ring Oscillators," IEEE Electron Device Letters EDL-6:359-362 (July 1985).

30. Ketterson, A., F. Ponse, T. Henderson, J. Klem, and H. Morkoc. "Extremely Low Contact Resistances for AlGaAs/GaAs Modulation-Doped Field-Effect Transistor Structures," Journal of Applied Physics 57: 2305-2307 (15 March 1985).

31. Lee, K., M. Shur, T. Drummond, and H. Morkoc. "Parasitic MESFET in (Al,Ga)As/GaAs Modulation Doped FET's and MODFET Characterization," IEEE Transactions on Electron Devices ED-31:29-35 (January 1984).

32. Lee, K., M. Shur, T. Drummond, and H. Morkoc. "Low Field Mobility of 2-D Electron Gas in Modulation Doped AlGaAs/GaAs Layers," Journal of Applied Physics 54:6432-6438 (November 1983).

33. Lee, K., M. Shur, T. Drummond, and H. Morkoc. "Electron density of the Two-Dimensional Electron Gas in Modulation doped Layers," Journal of Applied Physics 54:2093-2096 (April 1983).

34. Lee, K., M. Shur, T. Drummond, S. Su, W. Lyons, R. Fischer, and H. Morkoc. "Design and Fabrication of High Transconductance Modulation-Doped (AlGa)As/GaAs FETs," Journal of Vacuum Science Technology B1(2):186-189 (April-June 1983).

35. Lee, K., M. Shur, T. Drummond, and H. Morkoc. "Current-Voltage and Capacitance Characteristics of Modulation-Doped Field-Effect Transistors," IEEE Transactions on Electron Devices ED-30:207-212 (March 1983).

36. Lin, B., D. Tsui, M Paajanen, and A. Gossard. "Mobility of the Two-Dimensional Electron Gas in GaAs-AlGaAs Heterostructures," Applied Physics Letters 45:695-697, (15 Sep 1984).

37. Linh, N., P. Tung, D. Delegbeaudeuf, P. Delescluse, and M. Laviron. "High Speed-Low Power GaAs/AlGaAs TEGFET Integrated Circuit," Proceedings of 1982 International Electron Devices Meeting. 582-585 IEEE Press, New York, 1982.

38. Litton, C., Task Manager, Senior Scientist, Electronics 2Research Division, Air Force Avionics Laboratory. Personal interviews. Wright-Patterson AFB, OH, 1 March through 4 October 1985.

39. Luscher, P. "Crystal Growth by Molecular Beam Epitaxy," Solid State Technology 20(12):43-52 (December 1977).

40. Lyons, W., D. Arnold, R. Thorne, S. Su, W. Kopp, and H. Morkoc. "Normally-On and Normally-Off Camel Diode Gate GaAs and Modulation Doped GaAs/AlGaAs Field Effect Transistors," Institute of Physics Conference Ser. No. 65 Chapter 5:379-384, 1982.

41. Marlow, G., M. Das, and L. Tongson. "The Characteristics of Au-Ge-Based Ohmic Contacts to n-GaAs Including the Effects of Aging," Solid State Electronics 26(4):259-266 (1982).

42. Masselink, W., T. Drummond, J. Klem, W. Kopp, Y. Chang, F. Ponse, and H. Morkoc. "Saturation in the Transfer Characteristics of (Al,Ga)As/GaAs Modulation-Doped Field Effect Transistors at 77K," Applied Physics Letters 45:1190-1192 (1 December 1984).

43. McKelvey, John P. Solid State and Semiconductor Physics. New York, N.Y.: Harper & Row, 1966.

44. Mimura, T., S. Hiyamizu, T. Fujii, and K. Nanbu. "A New Field-effect Transistor with Selectively Doped GaAs/n-$Al_xGa_{1-x}As$ Heterojunctions," Japanese Journal of Applied Physics 19:L225-L227 (May 1980).

45. Moloney, M., F. Ponse, and H. Morkoc. "Gate Capacitance-Voltage Characteristic of MODFET's:Its Effect on Transconductance," IEEE Transactions on Electron Devices 32:1675-1684 (September 1985).

46. Morkoc, H. and P. Solomon. "The HEMT: a Superfast Transistor," IEEE Spectrum 21(2):28-35, (February 1984).

47. Morkoc, H., T. Drummond, and R. Fischer. "Interfacial Properties of (Al,Ga)As/GaAs Structures: Effect of Substrate Temperature During Growth By Molecular Beam Epitaxy," Journal of Applied Physics 53:1030-1033 (February 1982).

48. Morkoc, H. "Current Transport in Modulation Doped (Al,Ga)-As/GaAs Heterostructures: Applications to High Speed FET's," IEEE Electron Device Letters EDL-2:260-262 (October 1981).

49. Morkoc, H. "Modulation Doped GaAs/$Al_xGa_{1-x}As$ Layered Structures with Applications to Field Effect Transistors," DTIC Report AD-A126-392 (15 February 1982).

50. Nathan, M. and M. Heiblum. "An Improved AuGe Ohmic Contact to n-GaAs," Solid State Electronics 25:1063-1065 (October 1982).

51. Ogawa, M. "Alloying Behavior of Ni/Au-Ge Films on GaAs," Journal of Applied Physics 51:406-412 (January 1980).

52. Ohata, K., H. Hida, H. Miyamoto, M. Ogawa, T. Baba, and T. Mizutani. "A Low Noise AlGaAs/GaAs FET With P+-Gate and Selectively Doped Structure," 1984 IEEE MTT-S Digest. 434-436 (1984).

53. Pearah, P., T. Henderson, J. Klem, H. MOrkoc, B. Nilsson, O. Wu, W. Swanson, and D. Ch'en. "Rapid Thermal Annealing of Modulation-Doped $Al_xGa_{1-x}As$/GaAs Heterostructures for Device Applications," Journal of Applied Physics 56:1851-1855 (15 September 1984).

54. Ponse, F., W. Masselink, and H. Morkoc. "Quasi-Fermi Level Bending in MODFET's and Its Effect on FET Transfer Characteristics," IEEE Transactions on Electron Devices ED-32:1017-1023 (June 1985).

55. Rideout, V.L. "A Review of the Theory and Technology for Ohmic Contacts to Group III-V Compound Semiconductors," Solid State Electronics 18:541-550 (1975).

56. Roy, S., and A. Daw. "Effect of the Presence of an Inversion Layer in an MPN Structure," Solid State Electronics 25:169-173 (February 1982).

57. Shannon, J. "Control of Schottky Barrier Height Using Highly Doped Surface Layers," Solid State Electronics 19:537-543 (June 1976).

58. Sheng, N., C. Lee, R. Chen and D. Miller. "GaAs/AlGaAs Double Heterostructure High Electron Mobility Transistors," Proceedings of the 1984 International Electron Devices Meeting. 352-355. IEEE Press, New York, 1984.

59. Solomon, P., and H. Morkoc. "Modulation-Doped GaAs/AlGaAs Heterojunction Field-effect Transistors (MODFET's), Ultrahigh-Speed Device for Supercomputers," IEEE Transactions on Electron Devices ED-31:1015-1027 (August 1984).

60. "Speed Record Claimed for GaAs Transistor," Electronics Week 58(19):19-20 (13 May 1985).

61. Stern, F., and S. Das Sarma. "Electron Energy Levels in GaAs-$Ga_{1-x}Al_xAs$ Heterojunctions," Physical Review B 30:840-848 (15 July 1984).

62. Stoermer, H., A. Pinczuk, A. Gossard, and W. Wiegmann. "Influence of an Undoped (AlGa)As Spacer on Mobility Enhancement in GaAs-(AlGa)As Superlattices," Applied Physics Letters 38:691-693 (1 May 1981).

63. Stoermer, H., R. Dingle, A. Gossard, W. Wiegmann, and M. Sturge. "Two-Dimensional Electron Gas at a Semiconductor-Semiconductor Interface," Solid State Communications 29:705-709 (March 1979).

64. Szabo, Karl. "Fabrication and I-V Characterization of MODFETS Using Substrates Grown by Molecular Beam Epitaxy Using Solid Arsenic Sources," MS Thesis. School of Engineering, Air Force Institute of Technology (AU), Wright-Patterson A.F.B., Ohio (December 1984).

65. Thorne, R., S. Su, R. Fischer, W. Kopp, W. Lyons, P. Miller, and H. Morkoc. "Analysis of Camel Gate FET's (CAMFETs)," IEEE Transactions on Electron Devices ED-30:212-216 (March 1983).

66. Thorne, R., T. Drummond, W. Lyons, R. Fischer, and H. Morkoc. "An Explanation for Anomalous Donor Activation Energies in $Al_{0.35}Ga_{0.65}As$," Applied Physics Letters 41:189-191 (July 1982).

67. Tomizawa, M., A. Yoshii, and K. Yokoyama. "Modeling for an AlGaAs/GaAs Heterostructure Device Using Monte Carlo Simulation," IEEE Electron Device Letters EDL-6:332-334 (July 1985).

68. Tsui, D., and R. Logan. "Observation of Two-Dimensional Electrons in LPE-Grown GaAs-$Al_xGa_{1-x}As$ Heterojunctions," Applied Physics Letters 35:99-101 (15 July 1979.

69. Valois, A., and G. Robinson. "Deep Levels in AlGaAs/GaAs Modulation-Doped Structures Grown by MBE," Sixth Annual Molecular Beam Epitaxy Workshop. To be published. (August 1985).

70. Valois, A., G. Robinson, K. Lee, and M. Shur. "Temperature Dependence of the I-V Characteristics of Modulation-Doped FETs," Journal of Vacuum Science Technology B1(2):190-195, (April-June 1983).

71. Van Der Ziel, A. "Metal P-N Schottky Barrier Diodes," Solid State Electronics 20:269-272 (1977).

72. Vinter, B. "Phonon-Limited Mobility in AlGaAs/GaAs Heterostructures," Applied Physics Letters 45(5):581-582 (1 September 1984).

73. Vinter, B. "Subbands and Charge Control in a Two-Dimensional Electron Gas Field-Effect Transistor," Applied Physics Letters 44(3):307-309 (1 February 1984).

74. Waldrop, J. "Schottky-Barrier Height of Ideal Metal Contacts to GaAs," Applied Physics Letters 44(10):1002-1004 (15 May 1984).

75. Witkowski, L., T. Drummond, S. Barnett, H. Morkoc, A. Cho, and J. Greene. "High Mobility GaAs-$Al_xGa_{1-x}As$ Single Period Modulation-Doped Heterojunctions," Electronics Letters 17:126-128 (5 February 1981).

76. Williams, R. Gallium Arsenide Processing Techniques. Dedham, MA, Artech House, 1984.

VITA

Lieutenant Kevin L. Priddy was born on 23 December 1955 at Patuxent River NAS, Maryland. He is married and has three children. He graduated from high school in North Fort Myers, Florida, in 1974. Upon graduation he served in the Army for five years before entering Brigham Young University in 1979. He received the degree of Bachelor of Science in Electrical Engineering in April, 1982. Upon graduation he received his commission in the USAF and reported to Langley AFB, Virginia in May 1982. He served at Langley AFB as a staff officer until entering the School of Engineering, Air Force Institute of Technology, in May 1984.

Permanent address: 3336 N. Key Drive Apt. J-6
N. Fort Myers, FL 33903

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE

AD-A164103

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION: UNCLASSIFIED	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT: Approved for public release; distribution unlimited.
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S): AFIT/GEO/ENG/85D-1	5. MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION: School of Engineering; 6b. OFFICE SYMBOL (If applicable): AFIT/ENG	7a. NAME OF MONITORING ORGANIZATION
6c. ADDRESS (City, State and ZIP Code): Air Force Institute of Technology, Wright-Patterson AFB, Ohio 45433	7b. ADDRESS (City, State and ZIP Code)
8a. NAME OF FUNDING/SPONSORING ORGANIZATION: Electronic Research Div; 8b. OFFICE SYMBOL (If applicable): AFWAL/AADR	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c. ADDRESS (City, State and ZIP Code): Air Force Avionics Laboratory, Wright-Patterson AFB, Ohio 45433	10. SOURCE OF FUNDING NOS. — PROGRAM ELEMENT NO. / PROJECT NO. / TASK NO. / WORK UNIT NO.
11. TITLE (Include Security Classification): See Box 19	
12. PERSONAL AUTHOR(S): Kevin L. Priddy, B.S., 1 Lt, USAF	
13a. TYPE OF REPORT: MS Thesis; 13b. TIME COVERED: FROM _____ TO _____; 14. DATE OF REPORT (Yr., Mo., Day): 1985 December; 15. PAGE COUNT: 151	
16. SUPPLEMENTARY NOTATION	

17 COSATI CODES		
FIELD	GROUP	SUB. GR.
09	01	

18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number): Field Effect Transistors, Semiconductor Devices, Schottky Barrier Devices, High Electron Mobility Transistor, Modulation Doped Field Effect Trans.

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

Title: STUDY AND ANALYSIS OF AlGaAs/GaAs MODULATION DOPED FIELD EFFECT TRANSISTORS INCORPORATING P-TYPE SCHOTTKY GATE BARRIERS

Thesis Advisor: Donald R. Kitchen, Major, USAF
Instructor, Department of Electrical Engineering

Approved for public release: IAW AFR 190-1.
LYNN E. WOLAVER 16 JAN 86
Dean for Research and Professional Development
Air Force Institute of Technology (AU)
Wright-Patterson AFB OH 45433

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT: UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT. ☐ DTIC USERS ☐	21. ABSTRACT SECURITY CLASSIFICATION: UNCLASSIFIED
22a. NAME OF RESPONSIBLE INDIVIDUAL: Donald R. Kitchen, Major, USAF	22b. TELEPHONE NUMBER (Include Area Code): 513-255-4960; 22c. OFFICE SYMBOL: AFIT/ENG

DD FORM 1473, 83 APR EDITION OF 1 JAN 73 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE

The design and dc performance of enhanced Schottky barrier modulation doped transistors (ESMODFETs) is presented. The theory required to estimate the layer thicknesses and dopings required for a desired barrier height is developed. The experimental results show an increase from 0.8eV to 1.6eV for the ESMODFET versus the standard MODFET, with good correlation between theory and experiment. The ohmic contact resistance of the ESMODFET is comparable to that of the MODFET. The process used to fabricate the ESMODFET is similar to that used for the MODFET.

END

FILMED

3-86

DTIC